



CE65H160DNGI

CoreGaN 650V GaN HEMT

Description

The CE65H160DNGI Series 650V, 160mΩ gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic onresistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Automotive

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

Easy to drive—compatible with standard gate drivers

Low conduction and switching losses

RoHS compliant and Halogen-free

Benefits

Increased efficiency through fast switching

Increased power density

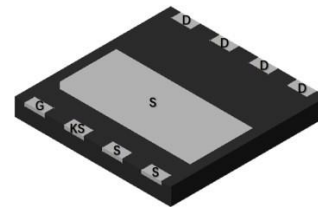
Reduced system size and weight

Ordering Information

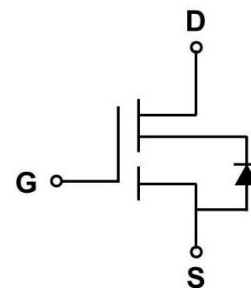
Part Number	Package	Package Configuration
CE65H160DNGI	DFN 8*8	Source



Top



Bottom



Circuit Symbol

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
650V	160mΩ	16A	7.2nC



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Limit value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650		
$V_{(TR)DSS}$	Drain to source voltage-transient ^a	900	V	
V_{GSS}	Gate to source voltage	-20~+20		
I_D	Continuous drain current @ $T_C=25^\circ\text{C}$ ^b	16	A	
	Continuous drain current @ $T_C=125^\circ\text{C}$ ^b	7		
I_{DM}	Pulse drain current (pulse width: 100 μs)	55	A	
P_D	Maximum power dissipation @ $T_C=25^\circ\text{C}$	78	W	
T_C	Operating temperature	Case	-55~150	$^\circ\text{C}$
T_J		Junction	-55~150	$^\circ\text{C}$
T_S	Storage temperature	-55~150	$^\circ\text{C}$	

a. In off-state, spike duty cycle $D<0.01$, spike duration $<1\mu\text{s}$

b. For increased stability at high current operation



Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	1.6	$^{\circ}\text{C} / \text{W}$



Electrical Parameters

T_J=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{(BL)DSS}	Drain-source voltage	650	-	-	V	V _{GS} = 0V
V _{GS(th)}	Gate threshold voltage	-	1.9	-	V	V _{DS} =1V, I _{DS} =1mA
ΔV _{GS(th)/T_J}	Gate threshold voltage temperature coefficient	-	-7	-	mV/°C	
R _{DS(on)}	Drain-source on-resistance	-	160	190	mΩ	V _{GS} =10V, I _D =1A, T _J =25°C
		-	340	-		V _{GS} =10V, I _D =1A, T _J =150°C
I _{DSS}	Drain-to-source leakage current	-	-	10	μA	V _{DS} =650V, V _{GS} = 0V, T _J =25°C
		-	-	100		V _{DS} =650V, V _{GS} = 0V, T _J =150°C
I _{GSS}	Gate-to-source forward leakage current	-	-	±100	nA	V _{GS} = ±20V
C _{ISS}	Input capacitance	-	239	-	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	-	25	-		
C _{RSS}	Reverse capacitance	-	1.4	-		
Q _G	Total gate charge	-	7.2	-	nC	V _{DS} =400V, V _{GS} =0V to 10V, I _D =1A
Q _{GS}	Gate-source charge	-	2.1	-		
Q _{GD}	Gate-drain charge	-	0.9	-		
Q _{OSS}	Output charge	-	31	-	nC	V _{GS} =0V, V _{DS} =0V to 400V, f=1MHz
t _{D(on)}	Turn-on delay	-	6	-	ns	V _{DS} =400V, V _{GS} =0V to 10V, I _D =2.1A, R _{G-on(ext)} =6.8Ω, R _{G-off(ext)} =2.2Ω, L=250μH
t _R	Rise time	-	17	-		
t _{D(off)}	Turn-off delay	-	7	-		
t _F	Fall time	-	15	-		



Electrical Parameters

T_J=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V _{SD}	Source-Drain reverse voltage	-	2.5	-	V	V _{GS} =0V, I _{SD} =10A
t _{RR}	Reverse recovery time	-	14	-	ns	I _F =10A, V _{DD} =400V, dI _F /dt=165A/μs
Q _{RR}	Reverse recovery charge	-	6.5	-	nC	



Typical Characteristics

T_J=25°C unless otherwise stated

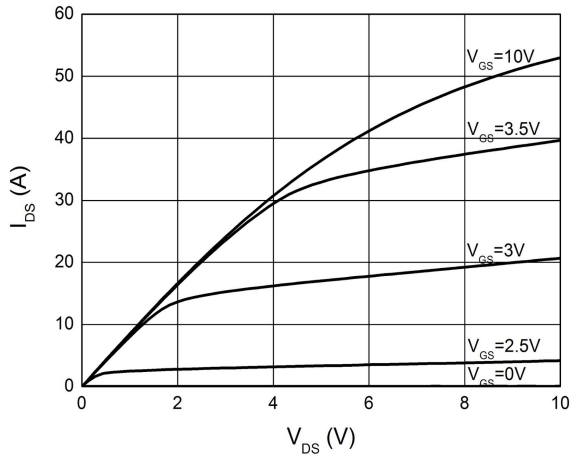


Figure 1. Typical Output Characteristics T_J=25°C

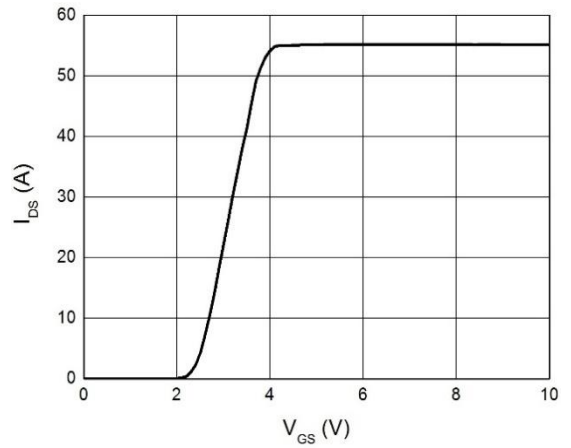


Figure 2. Typical Transfer Characteristics T_J=25°C (V_{DS}=10V)

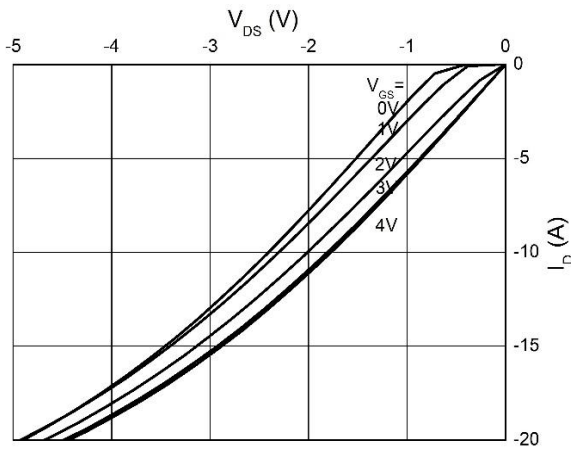


Figure 3. Channel Reverse Characteristics T_J=25°C

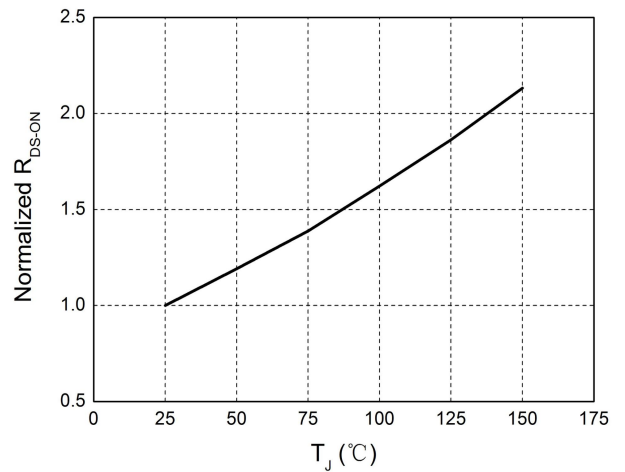


Figure 4. Normalized On-resistance



Typical Characteristics

$T_J=25^\circ\text{C}$ unless otherwise stated

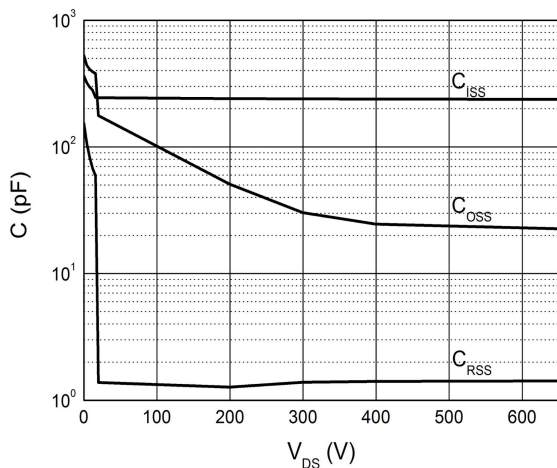


Figure 5. Typical Capacitance (f=1MHz)

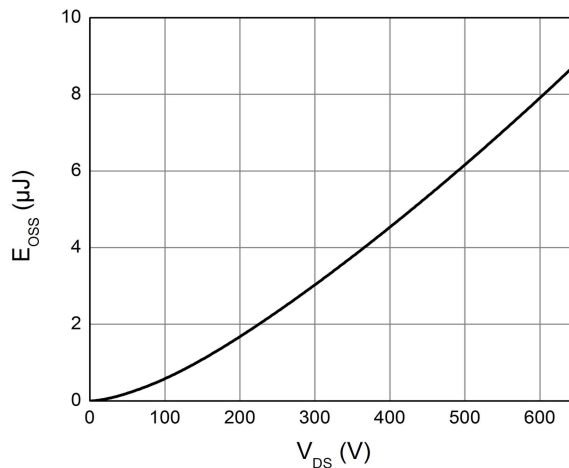


Figure 6. Typical C_{OSS} Stored Energy

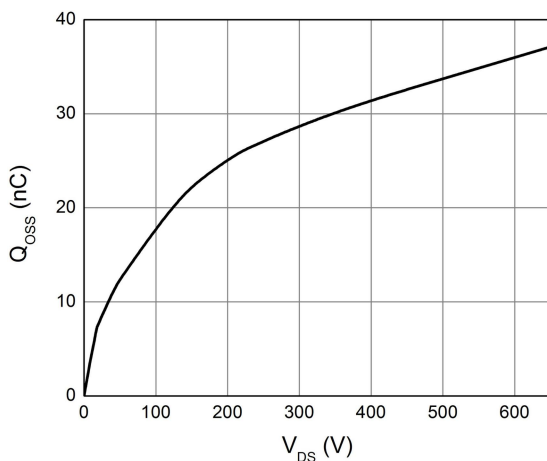


Figure 7. Typical Q_{OSS}

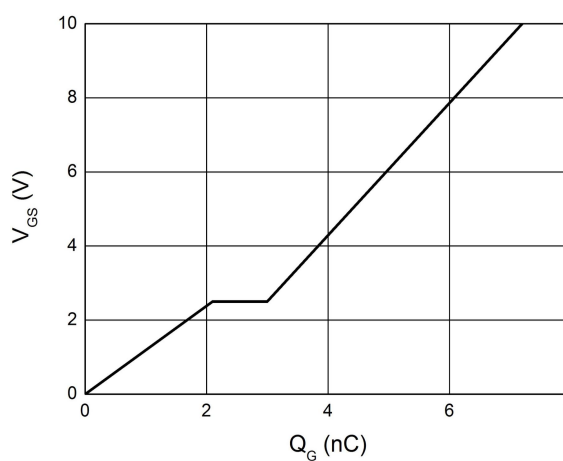


Figure 8. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)



Typical Characteristics

T_J=25°C unless otherwise stated

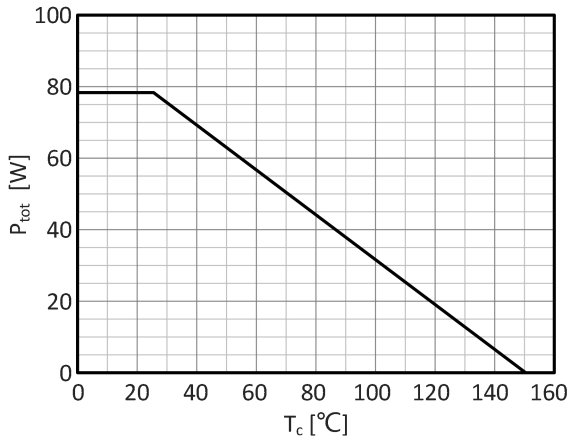


Figure 9. Power Dissipation

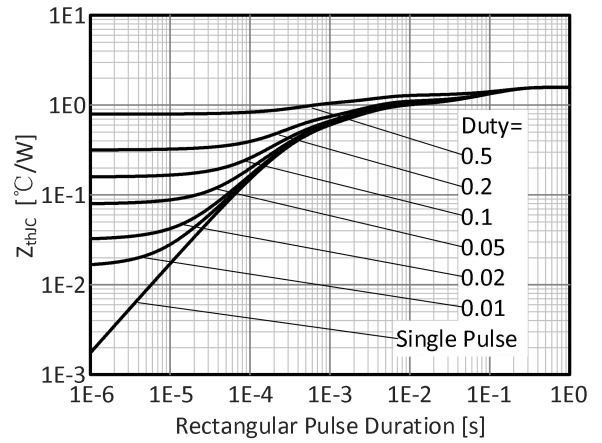


Figure 10. Transient Thermal Resistance

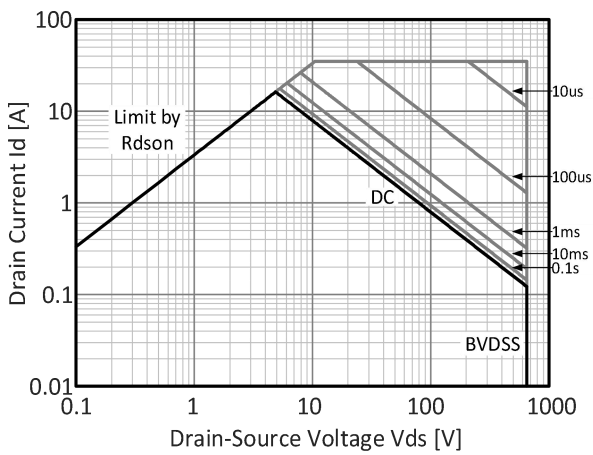


Figure 11. Safe Operating Area T_c=25°C

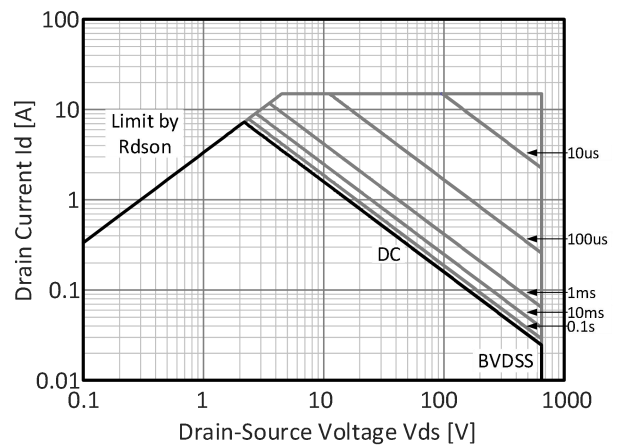


Figure 12. Safe Operating Area T_c=125°C

Typical Characteristics

$T_J=25^\circ\text{C}$ unless otherwise stated

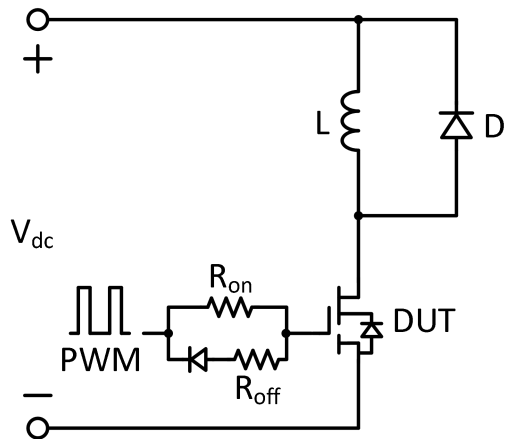


Figure 13. Switching times with inductive load

$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$ to 10V , $I_D=2.1\text{A}$,
 $R_{G-on(ext)}=6.8\Omega$, $R_{G-off(ext)}=2.2\Omega$, $L=250\mu\text{H}$

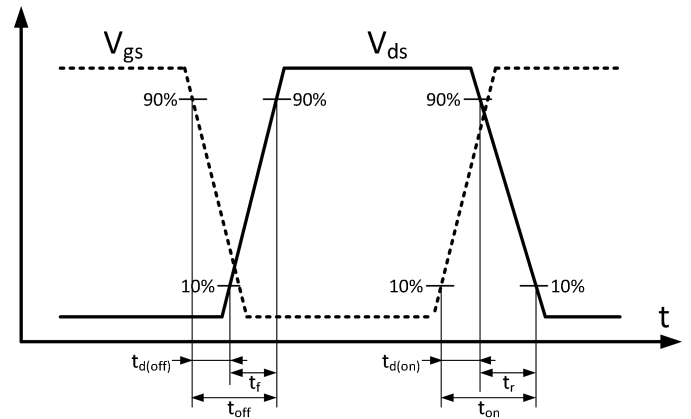


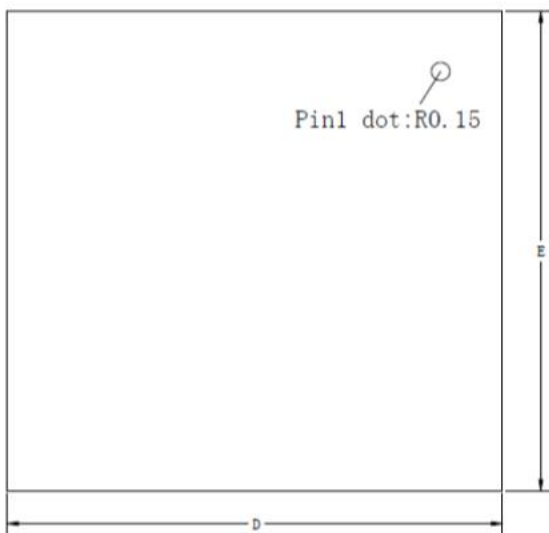
Figure 14. Switching times with waveform



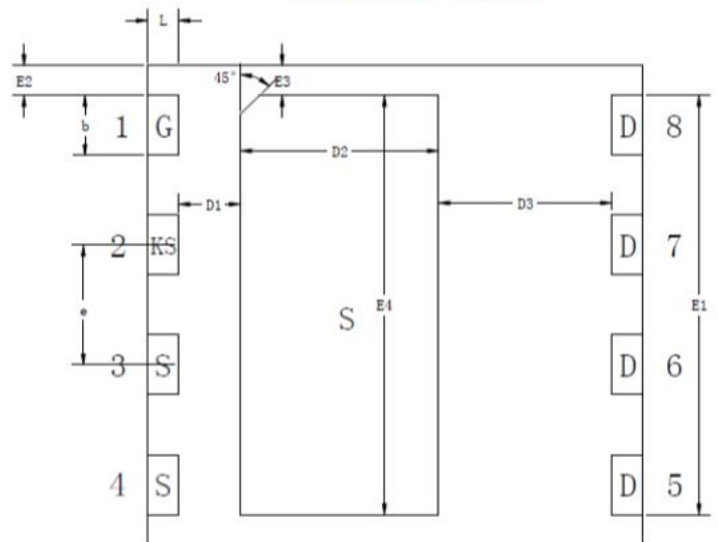
PACKAGE DIMENSIONS

DFN8x8-8L-1.10-A

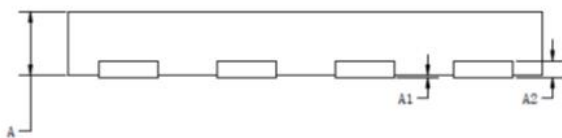
Top view



Bottom view



Side view(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	1.05	1.10	1.15
A1	0	0.02	0.05
A2	0.203REF		
D	7.9	8	8.1
E	7.9	8	8.1
D1	0.9	1	1.1
D2	3.1	3.2	3.3
D3	2.7	2.8	2.9
E1	6.9	7	7.1
E2	0.4	0.5	0.6
E3	0.4	0.5	0.6
E4	6.9	7	7.1
e	1.9	2	2.1
b	0.9	1	1.1
L	0.4	0.5	0.6