High-V_{TH} E-mode GaN HEMTs with Robust Gate-Bias-Dependent V_{TH} Stability Enabled by Mg-Doped *p*-GaN Engineering

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***Abstract*—Highly stable threshold voltage (V_{TH}) characteristics are an essential reliability requirement for *p*-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs) to withstand various gate bias stresses for power applications. In this work, we demonstrate high-V_{TH} (3.0 V) *p*-GaN HEMTs with robust V_{TH} stability by *p*-GaN gate engineering via Mg doping and activation. The V_{TH} degradation rates of the resulting device under both pulsed-*I*/*V* and bias temperature instability (BTI) stress conditions are less than 10% at high temperatures up to 150 °C, which is much lower than that of conventional Schottky-type *p*-GaN HEMTs (20%~30%). Such notable V_{TH} characteristics are due to the impact ionization-dependent hole compensation under certain gate stress, which effectively alleviates the electron trapping effect and reduces positive V_{TH} shift. The impact ionization occurring in fully depleted *p*-GaN layer has been confirmed by both positive temperature-dependent gate breakdown characteristics and numerical simulations. Furthermore, shallow- and deep-level hole traps are identified in the gate stack of high-V_{TH} devices by performing deep-level transient spectroscopy (DLTS) technique. Consequently, the trapping effect associated with hole traps may also alleviate the undesired electron-trapping-induced V_{TH} shift. These results provide critical understandings on the V_{TH} stability of the high-V_{TH} *p*-GaN HEMTs and important design guidance for commercial device development.**

***Index Terms*—*p*-GaN HEMT, V_{TH} stability, impact ionization, hole trap, gate bias stress.**

I. Introduction

GALLIUM nitride (GaN)-based power devices, especially *p*-GaN/AlGaN/GaN high-electron-mobility transistors (*p*-GaN HEMTs), have gained huge popularity in recent years due to their superior material and structure properties [1]-[7]. For *p*-GaN HEMTs, the rational design of gate *p*-GaN layer grown on AlGaN layer is critical to realize normally-off operation with positive threshold voltage (V_{TH}) characteristics. In general, the construction of *p*-GaN layers involves Mg doping and activation [4], [8], as well as the associated growth/annealing temperature and concentration considerations [9], which are complex *p*-GaN gate engineering for balancing process compatibility and device performance. Most importantly, due to the Mg out-diffusion from *p*-GaN into underlying layer and the nature of the "floating *p*-GaN layer" sandwiched between gate and channel [10], the V_{TH} of normal *p*-GaN HEMTs is usually limited to 1.2~1.5 V, otherwise the ON-state characteristics (e.g., ON-resistance) will be deteriorated. Under high-frequency and high-power conditions, gate ringing could easily exceed this low V_{TH} and lead to false turn-on, compromising device ruggedness and reliability. Furthermore, the gate bias-induced carrier impact ionization (I. I.) and the trap distribution involved in the gate stack strongly depend on the *p*-GaN gate engineering, which have not been systematically studied. Therefore, while the maturity of *p*-GaN gate engineering technique signifies the

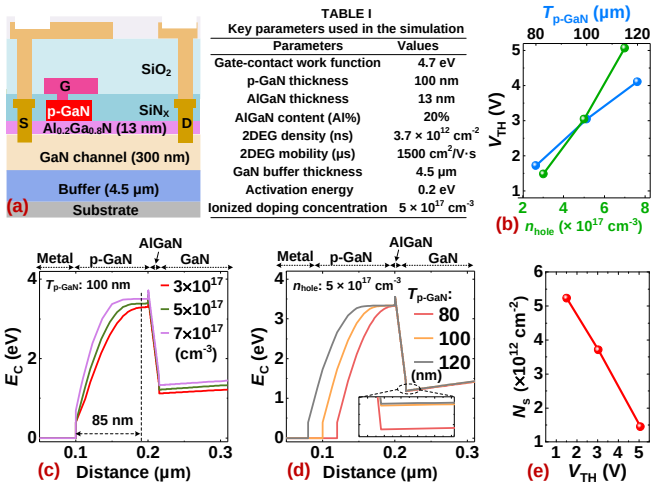

Fig. 1. (a) Schematic cross-sectional of the HV$_T$-HEMT. (b) Simulated V_{TH} against n_{hole} and $T_{p\text{-}GaN}$. Conduction band energy profiles along gate stack with different (c) n_{hole} and (d) $T_{p\text{-}GaN}$. (e) N_S versus V_{TH}.

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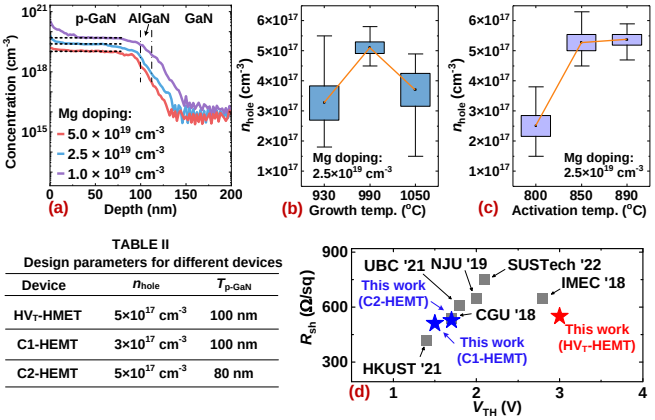

TABLE II
Design parameters for different devices

Device	n_{hole}	$T_{p\text{-}GaN}$
HV_T-HMET	5×10^{17} cm^{-3}	100 nm
C1-HEMT	3×10^{17} cm^{-3}	100 nm
C2-HEMT	5×10^{17} cm^{-3}	80 nm

Fig. 2. (a) Mg-depth profiles with different doping comcentrations. Effect of (b) p-GaN growth temperature and (c) activation temperature on n_{hole}. (d) Comparison of R_{sh} and V_{TH} of the *p*-GaN HEMTs.

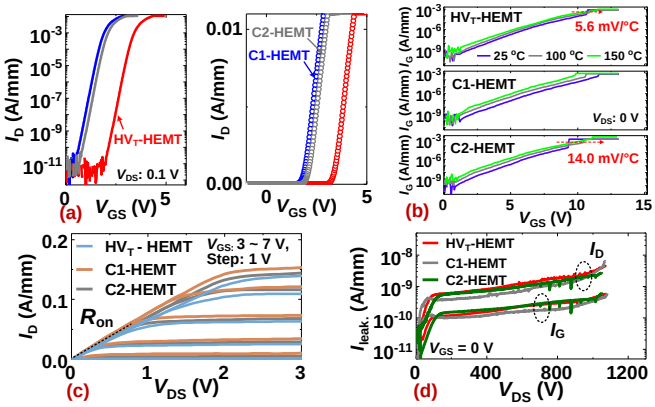

Fig. 3. (a) Transfer curves of the HVT-, C1- and C2-HEMTs in log scale- and linear-scale. (b) Temperature-dependent gate breakdown curves. (c) Output and (d) OFF-state breakdown characteristics.

practical manufacturability of GaN-based normally-off power devices, the performance trade-offs (e.g., V_{TH} versus R_{on}) have not yet been fully realized, and the underlying mechanism for sustaining V_{TH} stability has not been explored.

In particular, the V_{TH} instability induced by the "floating *p*-GaN layer" would severely deteriorate gate stability and reliability. The V_{TH} shift value of the *p*-GaN HEMTs generally reaches 0.3 ~ 0.5 V under certain gate stresses [8]-[11], and considering a normal V_{TH} of 1.2~1.5 V, the resulting V_{TH} degradation rate ($|\Delta V_{TH}|/V_{TH,0}$) is as high as 20% ~ 30%. Such degradation of V_{TH} characteristics is a formidable challenge for the further development of *p*-GaN gate HEMT technology.

In this work, based on the *p*-GaN gate engineering technique, we have systematically investigated the effect of hole concentration and *p*-GaN thickness on the device's V_{TH} characteristics. With Mg doping and *p*-GaN activation optimized by simulations and process experiments, the resulting high-V_{TH} device exhibits a good trade-off between V_{TH} and R_{on}. Moreover, the V_{TH} degradation rates of such device under pulsed-*I/V* and bias temperature instability (BTI) stress are only 0.4% and 8%, respectively. The I. I.-induced hole compensation mechanism is identified as the dominant for sustaining V_{TH} stability. Furthermore, the trap properties in the gate stack are investigated by performing DLTS tests.

II. Gate Stack Simulation and Static Characteristics

A. V_{TH} Simulations and *p*-GaN Optimization

Fig. 1(a) shows the schematic of the high-V_{TH} *p*-GaN HEMT (HV_T-HEMT) structure grown by metal-organic chemical vapor deposition on a 6-inch silicon substrate. The effect of the *p*-GaN design parameters [i.e., hole concentration (n_{hole}) and thickness ($T_{p\text{-}GaN}$)] on the V_{TH} are first investigated using numerical simulations. The main parameters used for simulation calibration are depicted in Table I. The incomplete ionization model with a activation energy of 0.2 eV is adopted to calibrate the ionized doping concentration [12], while taking into account other numerical models such as *GaNsat.n*, *selb*, *lat.temp*, *consrh*, *auger*, *albrct.p*, *ten.piezo*, *and calc.strain*. To further refine the models, the simulated transfer and output curves as well as two-dimensional electron gas density (n_s) are extracted for comparison and calibration with experimental results. Fig. 1(b) shows the simulated V_{TH} against n_{hole} and $T_{p\text{-}GaN}$. With n_{hole} increasing from 3×10^{17} to 7×10^{17} cm^{-3} or $T_{p\text{-}GaN}$ changing from the 80 to 120 nm, the device exhibits an improved V_{TH} from 1.5~1.7 V to 4.1~5.2 V. This increased V_{TH} can be understood from the conduction energy band diagram of the *p*-GaN gate stack [Fig. 1(c) and (d)]. Under unbiased equilibrium condition of the *p*-GaN gate with a n_{hole} of 5×10^{17} cm^{-3} and a $T_{p\text{-}GaN}$ of 100 nm, the depletion region of the Schottky junction has a width of ~85 nm, which is close to the value (~82 nm) calculated by the one-sided metal-semiconductor junction model [13]. The conduction band at the AlGaN/GaN interface shifts upward with increasing n_{hole} or $T_{p\text{-}GaN}$, thus leading to a decrease in n_s [Fig. 1(e)] and an increase in V_{TH}. Note that the 100-nm-$T_{p\text{-}GaN}$ *p*-GaN layer should be fully depleted under certain gate bias [13], where the electric field (*E*-field) and I. I. rate will be discussed in the section IV.

The desired n_{hole} is highly dependent on Mg doping and activation during *p*-GaN growth, where the inevitable atomic out-diffusion associated with Mg dopants could affect the V_{TH} and R_{on}. The experimental Mg-depth profiles with different doping concentrations are shown in Fig. 2(a), as measured by secondary ion mass spectrometry (SIMS). The Mg out-diffusion from *p*-GaN into underlying AlGaN/GaN layer is effectively suppressed as the doping concentration decreases, and the lower doping concentration also contributes to minimizing the Mg spikes that often occur at the initial stage of *p*-GaN growth due to memory effect of Mg atoms [1]. However, lower Mg doping concentration is accompanied by a decrease in n_{hole} due to the limited acceptor ionization rate. By optimizing the *p*-GaN growth temperature [990 °C, Fig. 2(b)] and Mg activation temperature [850 °C, Fig. 2(c)], a laudable n_{hole} of ~5×10^{17} cm^{-3} can be obtained with a Mg doping concentration of ~2.5×10^{19} cm^{-3}, delivering an acceptor ionization rate of ~2%, which is higher than previously reported results (1%~1.3%) [13], [14]. By further adjusting the *p*-GaN growth temperature to 920 °C and the activation temperature to 830 °C, a control device (C1-HEMT) with a low n_{hole} of ~3×10^{17} cm^{-3} can be realized. To enable a comprehensive comparison, another control device (C2-HEMT) with 80-nm $T_{p\text{-}GaN}$ is also fabricated. The *p*-GaN design parameters for the three types of devices are listed in Table II. These devices are fabricated on a 6-inch process platform, with a detailed process flow illustrated in our

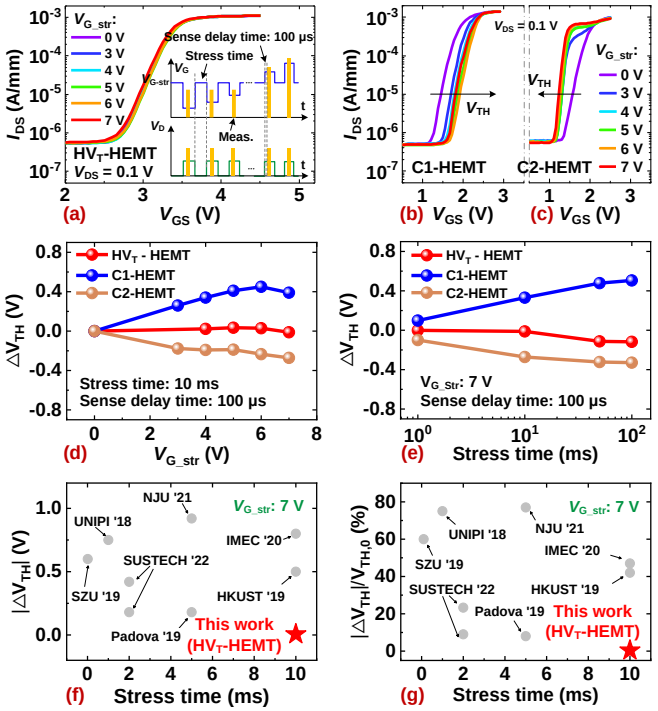

Fig. 4. Transfer curves of the (a) HV_T-, (b) C1- and (c) C2-HEMTs under pulsed-*I/V* stresses. Extracted ΔV_{TH} of three types of devices with different (d) V_{G_str} and (e) t_{G_str}. Comparison of (f) $|\Delta V_T|$ and (g) its degradation rate ($|\Delta V_T|/V_{T,0}$) with the state-of-the-art *p*-GaN HEMTs.

previous work [15]. The fabricated devices feature a gate length (width) of 1.5 μm (90 mm) and a gate-to-source (gate-to-drain) distance of 3 μm (19 μm). The extracted sheet resistance (R_{sh}) and n_s of the HV_T-HEMT are 550 Ω/sq and 3.7 × 10^{12} cm^{-2}, respectively, while those of the C1-HEMT are (511 Ω/sq, 5.2 × 10^{12} cm^{-2}) and the C2-HEMT are (528 Ω/sq, 4.8 × 10^{12} cm^{-2}). Accordingly, R_{sh} and n_s for HV_T-HEMT did not degrade significantly, which should be attributed to the effectiveness of *p*-GaN gate engineering via Mg doping and activation. Fig. 2(d) shows the R_{sh}-V_{TH} comparison between HV_T-HEMT and the reported results [1]-[6].

B. Gate Breakdown and Static I-V Characteristics

Fig. 3(a) and (b) shows the DC transfer and gate breakdown characteristics of the three types of devices, respectively. Apparently, the HV_T-HEMT exhibits a high V_{TH} of 3.0 V at a drain current (I_D) of 10 μA/mm (3.4 V by linear extrapolation) [4], which is higher than that of C1-HEMT (1.5 V) and C2-HEMT (1.7 V). The gate breakdown voltages ($V_{G\text{-}BV}$) of HV_T-, C1- and C2-HEMTs are 10.7, 11.6 and 9.3 V respectively. Meanwhile, with temperature increasing from 25 to 150 °C, the $V_{G\text{-}BV}$ of the HV_T-HEMT increase from 10.7 to 11.4 V, revealing that temperature-dependent I. I. occurs in the *p*-GaN gate due to thermally enhanced phonon scattering. Fig. 3(c) and (d) show the output and OFF-state breakdown characteristics of these devices, respectively. The R_{on} of the HV_T- and C1-HEMTs are 14.4 and 11.7 Ω·mm, respectively, while that of C2-HEMT is 13.3 Ω·mm. And similar breakdown voltages (1071~1075 V) are obtained for different devices, where the low gate leakage under reverse blocking condition indicates that the OFF-state leakage current is mainly dominated by the buffer leakage, which is determined by the high-resistance buffer epitaxy material and process [16].

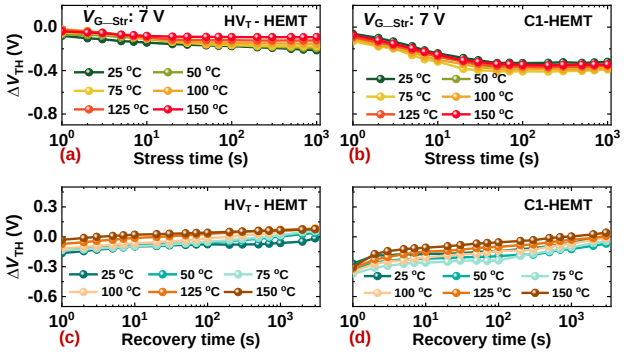

Fig. 5. (a), (b) Temperature-dependent ΔV_{TH} evolution under 1 ~ 1000 s PBTI stress, and (c), (d) subsequent 1 ~ 3000 s recovery.

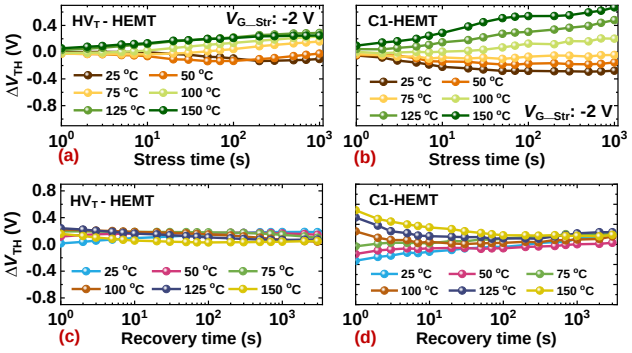

Fig. 6. (a), (b) Temperature-dependent ΔV_{TH} evolution under 1 ~ 1000 s NBTI stress, and (c), (d) subsequent 1 ~ 3000 s recovery.

III. V_{TH} Stability Characterizations

To comprehensively evaluate the V_{TH} stability of the devices, both pulsed-*I/V* and BTI stress tests have been conducted by a B1505 power device analyzer, with the high-current source measurement unit (HCSMU) applied on the drain and the medium-current source measurement unit (MCSMU) applied on the gate and source.

A. V_{TH} Stability in Pulsed-I/V Characterizations

The schematic waveforms of the pulsed-*I/V* test are illustrated in Fig. 4(a), including gate stress phase and subsequent transfer characteristic measurement phase. During the stress phase, constant-voltage gate bias (V_{G_str}) is applied to the device with source and drain terminals tied to the ground. After a certain time (t_{G_str}) of gate bias with fixed sense delay time of 100 μs, the V_{TH} of the device is extracted by executing the I_D-V_G measurements with a V_{DS} of 0.1 V. This low V_{DS} could rule out the possible trapping effect induced by the drain-applied stress [8].

Fig. 4(a), (b) and (c) shows the pulsed-*I/V* characteristics of V_{TH} for the HV_T-, C1- and C2-HEMTs with t_{G_str} of 10 ms and various V_{G_str} from 0 to 7 V, respectively. The HV_T-HEMT shows a slight V_{TH} shift in the entire measured gate bias range, which is significantly different from the C1-HEMT with a large positive V_{TH} shift and the C2-HEMT with a high negative V_{TH} shift [10]. The corresponding V_{TH} shift values (ΔV_{TH}s) extracted from the pulsed-*I/V* curves are shown in Fig. 4(d). The ΔV_{TH} measured from the HV_T-HEMT is almost independent of V_{G_str}, whereas that of C1-HEMT keeps shifting positively over the bias range from 0 to 6 V. This bias-induced positive ΔV_{TH} behavior of the C1-HEMT is consistent

TABLE III
COMPARISON OF V_{TH} STABILITY OF *P*-GAN HEMTS UNDER BTI STRESS

Devices	Tem. (°C)	$\|\Delta V_{TH}\|$ (PBTI)	$\|\Delta V_{TH}\|/V_{TH,0}$ (PBTI)	$\|\Delta V_{TH}\|$ (NBTI)	$\|\Delta V_{TH}\|/V_{TH,0}$ (NBTI)
HV_T-HEMT (This work)	25	0.21	7%	0.10	3%
	150	0.09	3%	0.24	8%
C1-HEMT (This work)	25	0.32	21%	0.28	19%
	150	0.34	23%	0.67	45%
Ref. [8][2022]	25	0.23	11%	N/A	N/A
	50	0.16	8%	N/A	N/A
Ref. [18][2022]	20	N/A	N/A	0.22	18%
	30	N/A	N/A	0.40	33%

All BTI values are extracted at a stress time of 1000 s and a stress voltage of 6 ~ 7 V (PBTI) / -2 V (NBTI).

with previously reported results [8], which have been identified as electron trapping-related physical mechanisms, e.g. trapping in AlGaN/GaN interface or depleted *p*-GaN region [17]. With V_{G_str} further increasing from 6 to 7 V, the dependence of the ΔV_{TH} on V_{G_str} changes from the positive to negative (i.e. V_{TH} shows less positive shift), which is generally believed to be caused by hole accumulation at the *p*-GaN/AlGaN interface, hole trapping in the AlGaN layer, hole recombination with the electron and de-trapping of electrons [8]. The competition mechanism between electron and hole dynamics is responsible for the instability of V_{TH}, and the apparent positive V_{TH} shift in C1-HEMT implies that the electron trapping effect is more dominant under various pulsed V_{G_str} [Fig. 4(d)] and t_{G_str} [Fig. 4(e)] conditions. Differently, the V_{TH} of C2-HEMTs shifts negatively, revealing a hole-dominated V_{TH} shifting mechanism [10].

Notably, the HV_T-HEMT exhibits robust V_{TH} stability under various stress conditions [Fig. 4(d) and (e)]. With a high V_{G_str} of 7 V and a t_{G_str} of 10 ms, the device shows an extremely small V_{TH} degradation rate ($|\Delta V_{TH}|/V_{TH,0}$) of 0.4%, which is much lower than that in the state-of-the-art *p*-GaN HEMTs [Fig. 4(f) and (g)] [10]-[17]. To our knowledge, this is the first demonstration of the High-V_{TH} *p*-gate HEMT with superior V_{TH} stability suitable for power applications.

B. V_{TH} Stability in BTI Characterizations

To gain further insight into the V_{TH} evolution of the device under gate bias stress, long-term BTI tests with a typical *measure-stress-measure* sequence (including gate stress and recovery phases) have been conducted. Fig. 5(a) and (b) show the ΔV_{TH} values of the HV_T- and C1-HEMTs measured with positive BTI (PBTI) stress time from 1 to 1000 s and temperatures from 25 to 150 °C at a high stress voltage of 7 V. For different test temperatures, it is found that all ΔV_{TH}s reach saturation within hundreds of seconds [8], after which the V_{TH} shows less negative shift (i.e. $|\Delta V_{TH}|$ decreases) with increasing temperature. The V_{TH} shift behavior is more prominent under long-term PBTI stress conditions, suggesting that carrier dynamics are affected by prolonged stress duration. On the other hand, a negative gate bias of -2 V is chosen as the stress voltage for negative BTI (NBTI) tests, since -1 ~ -3 V is usually used to suppress gate ringing in high frequency switching applications. Fig. 6 shows the temperature-dependent NBTI characteristics of the HV_T- and C1-HEMTs.

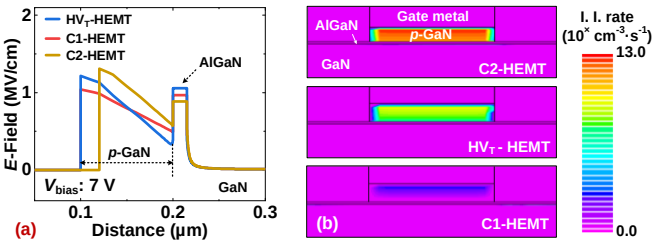

Fig. 7. (a) The simulated *E*-field distribution in the gate stack region of three types of devices, and (b) the corresponding I. I. rate.

Note that the Schottky junction in the gate stack is forward biased when negative bias is applied to the gate [18]. At 25 °C, the V_{TH} of the device first shifts negatively, and then shifts from negative to positive with temperature varying from 25 to 150 °C. The long-term negative bias stress combined with the high temperature is expected to lower the energy barrier between *p*-GaN and AlGaN layers [18], [19]. Resultantly, the electrons could "spill-over" from the 2DEG channel to the *p*-GaN layer and interact with holes, presenting an increased positive V_{TH} shift. Such electron-injection-induced positive V_{TH} degradation behavior is more severe for C1-HEMT, as shown in Fig. 6(b).

In summary, the HV_T-HEMT exhibits more stable V_{TH} characteristics than C1-HEMT under BTI stresses (Fig. 5 and 6). Whereas the C2-HEMT exhibits a severe negative V_{TH} shift (not shown here), being similar with the results observed from pulsed-*I/V* stresses. The comparison of the BTI characteristics of the HV_T-HEMT with the best prior reports is summarized in Table III. Even at 150 °C, the V_{TH} degradation rate under PBTI and NBTI stresses are only 3% and 8%. It is worth noting that these notable results are obtained under the BTI measurement conditions with time constants higher than 1 s [8], while under lower transient measurement conditions devices may exhibit evident V_{TH} shifts [11].

IV. MECHANISMS OF V_{TH} STABILITY

Compared with the C1- and C2-HEMTs, HV_T-HEMT exhibits superior V_{TH} stability. To reveal the physical mechanisms involved in V_{TH} shifts, *E*-field and I. I. simulations, DLTS experiments and gate leakage measurements have been carried out.

A. Hole generation induced by impact ionization

It has been proved that in the OFF-state drain breakdown events [20], with a certain *E*-field, I. I.-induced holes generation can effectively counteract electron trapping, thereby affecting the shift of electrical parameters. In this work, under a certain forward gate bias, the thin *p*-GaN in the gate stack is fully depleted due to the limited hole concentration caused by the low acceptor ionization rate. As a result, the peak *E*-field for gate breakdown within *p*-GaN is much lower than critical breakdown *E*-field of GaN (3.3 MV/cm), such as ~1.4 MV/cm as reported by Wu *et al.* [13]. In fact, the partial depletion of *p*-GaN with a high peak *E*-field can only be achieved with the extremely high active Mg concentrations (i.e., $n_{hole} > 10^{18}$ cm^{-3}) [19], while the current n_{hole}s are mostly in the range of 10^{16} ~ 10^{17} cm^{-3} [14]. With increasing forward gate bias, the peak *E*-field within *p*-GaN is gradually enhanced (although the value is still below 3.4

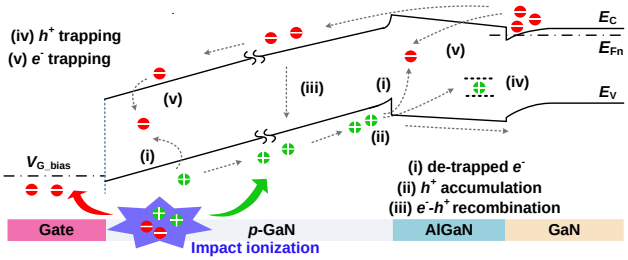

Fig. 8. Schematic band diagram along the gate stack of HV$_T$-HEMT with hole-assisted V_{TH} modulation process via impact ionization.

MV/cm), accompanied by the evolution of impact ionization. Specifically, the electrons in the channel could be emitted over the AlGaN barrier and injected into the *p*-GaN under a certain forward gate bias. The electrons transferred to *p*-GaN can be accelerated by the *E*-field in the depletion region, leading to the initiation of impact ionization. It has been reported that the I. I. within *p*-GaN is the most intense under gate breakdown transient, and a clear luminescence is observed due to the recombination of I. I.-produced electron-hole pairs [13]. For HV$_T$-HEMTs, the extracted I. I. rate and peak *E*-field are 10^9 cm^{-3}s^{-1} and 1.22 MV/cm (Fig. 7), respectively, both of which are higher than that in C1-HEMTs (10^3 cm^{-3}s^{-1}, 1.04 MV/cm). The relatively higher I.I. rate in HV$_T$-HEMT is believed to induce a certain amount of electron-hole pairs within *p*-GaN. For these carriers, electrons are bound to be swept away towards the forward-biased gate, while holes in the valence band drift towards the AlGaN layer [11]. The generated holes, on one hand, could assist the trapped electrons in the depleted *p*-GaN region and AlGaN layer de-trapping [21]. On the other hand, holes will accumulate at the *p*-GaN/AlGaN interface due to the band offset between the valence bands of *p*-GaN and AlGaN. Meanwhile, the holes can also recombine with electrons injected from the channel. Consequently, the enhanced hole-assisted electron de-trapping, hole accumulation/trapping and hole-electron recombination could effectively alleviate the V_{TH} shift caused by the electron trapping effect (Fig. 8). As noticeable, although the I. I. rate achieved in the HV$_T$-HEMT is not as high as that in the C2-HEMT (~10^{13} cm^{-3}s^{-1}), it is the most satisfactory result here. The excessive I. I. could lead to a large amount of holes generation and result in hole-dominated V_{TH} instability. Indeed, the C2-HMET exhibits an evident negative V_{TH} shift under gate stress [Fig. 4(d) and (e)]. Therefore, a moderate I. I. is highly desired, which contributes to relatively balanced charge distribution in the gate stack and sustains V_{TH} stability.

The positive temperature-dependent gate breakdown characteristics of the HV$_T$-HEMT reveal the drastic I. I. under breakdown transient, resulting in a sharp increase in gate leakage [Fig. 3(b)]. Correspondingly, the extracted *E*-field at 25 °C is 1.62 MV/cm, corresponding to a I. I. rate of 10^{17} cm^{-3}s^{-1}. Such high I. I. rate indicates a high level of hole generation and carrier recombination. Furthermore, the positive temperature coefficients of $V_{G\text{-}BV}$ are 5.6 mV/°C and 14.0 mV/°C for HV$_T$- and C2-HEMT, respectively. The higher positive temperature coefficient of C2-HEMT implies more severe phonon scattering and I. I., which is confirmed by simulations. The gate breakdown that occurs in fully depleted *p*-GaN may be due to the presence of Mg spikes on the upper surface of *p*-GaN, resulting in an enhanced local *E*-field at the

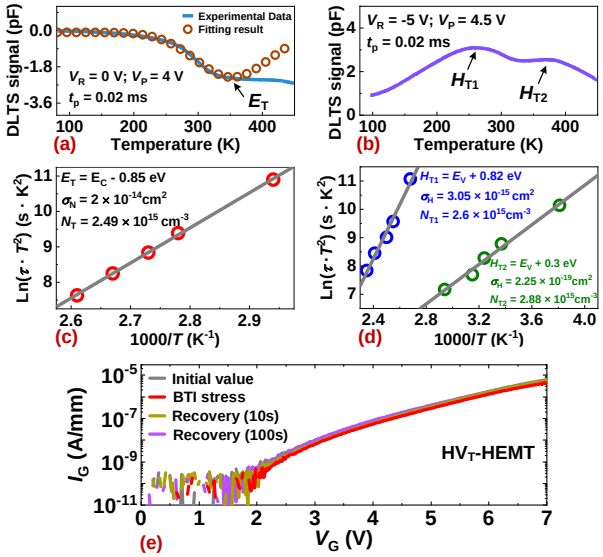

Fig. 9. Temperature-dependent DLTS spectra of p-i-n gate stack with detected (a) electron and (b) hole traps, and the corresponding trap levels, concentrations and capture cross sections are shown in (c) and (d), respectively. (e) Gate leakage characteristics of HV$_T$-HEMT.

Schottky junction under breakdown transient and thus affecting the breakdown ruggedness of the gate stack.

In addition, long-term BTI stress experiments show that the V_{TH} stability is not only affected by high temperature but also by prolonged stress duration [19]. Under BTI conditions, more energetic electrons in the 2DEG channel can overcome the AlGaN barrier and flow toward the gate [8]. Consequently, the hole-induced V_{TH} shift due to temperature/duration-dependent I. I. is in turn compensated by the enhanced electron trapping [Fig. 5 (a) and 6 (a)].

B. Trap extraction and analysis

Further investigation of trap properties in the gate stack of the HV$_T$-HEMT, especially deep level traps, can be revealed by employing DLTS measurements using a lock-in amplifier technique [22]. The DLTS signal detection is based on monitoring the capacitance changes (ΔC) induced by the temperature-dependent de-trapping (i.e., emission of carriers) of trap states within the space charge region of a reverse-biased junction. To investigate the Mg out-diffusion into the underlying layer and monitor the DLTS signal of the reverse-biased *p*-GaN/AlGaN/GaN (p-i-n) heterojunction, test samples with p-i-n structure (i.e., with Ni/Au ohmic gate contact) are prepared using the same *p*-GaN growth process as mentioned above. The measurement gate bias (V_R) is 0/-5 V with a pulse width (t_p) of 0.02 ms, while reverse filling pulse bias (V_p) is 4/4.5 V, and scanning temperature range is 80~450 K with a heating rate of 100 mK/s. Fig. 9(a) and (b) show the DLTS signals of electron trap and hole traps of the p-i-n heterojunction, respectively, where positive peaks related to hole traps can be clearly observed without fitting the data. Based on the DLTS spectra, two hole traps labeled as H_{T1}, H_{T2} with an activation energy (E_A) of 0.82 eV and 0.30 eV, and one electron trap labeled as E_T with an activation energy of 0.85 eV are deduced from the slopes of Arrhenius plot [22], and the corresponding trap concentration (N_T) and capture cross sections (σ) are also extracted from the plot of Ln ($t \cdot T^2$)) versus 1000/T [Fig. 9(c) and (d)]. The traps should be located

within AlGaN and/or GaN channel of the p-i-n heterojunction and deserves further investigation. Similar electron trap (E_T) and hole shallow-level trap (H_{T2}) are detected in C1-HEMT, which have also been observed in low-V_{TH} *p*-GaN HEMTs in previous work [23]. However, the deep-level hole trap (H_{T1}) obtained here in the gate stacks of HV_T- and C2-HEMTs has not been reported. The deep-level hole trap should be attributed to atom substitution/displacement caused by Mg out-diffusion during gate stack growth, resulting in donor-like Mg_{Ga} (gallium-site Mg) vacancies and related complexes (e.g. Mg_{Ga}-V_N complexes) [24], [25]. Together with the shallow-level hole traps observed in HV_T-HEMT, the capture of holes by trap states is more prominent under gate bias stress. As a result, the positive V_{TH} shift induced by electron trapping is most likely mitigated by the negative V_{TH} shift caused by hole trapping. Very recently, the hole-trapping assisted V_{TH} compensation mechanism has also been reported in p-n junction/AlGaN/GaN gate stack with specific interdiffusion region [8]. Note here that the trapping effects induced by Mg out-diffusion do not lead to permanent degradation of gate characteristics [26], which can be confirmed by gate leakage tests. The gate leakage current of the device decreased slightly under 7 V/1000 s BTI stress, probably due to the trap filling effect, and then returned to the initial value in the subsequent recovery duration [see Fig. 9(e)].

V. Conclusion

With the advantageous *p*-GaN gate engineering technique, the robust gate-bias-dependent V_{TH} stability has been demonstrated in the high-V_{TH} *p*-GaN HEMTs. In particular, the V_{TH} degradation rates of the devices under pulsed-*I/V* and BTI stress are only 0.4% and 8%, respectively. These results present the notable potentials of the high-V_{TH} *p*-GaN HEMTs with improved V_{TH} characteristics for high-voltage and high-temperature power switching applications.

References

[1] G. Zhou *et al*., "p-GaN Gate HEMTs With 10.6 V Maximum Gate Drive Voltages by Mg Doping Engineering," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2282-2286, Mar. 2022, doi: 10.1109/ted.2022.3157569.

[2] G. Zhou *et al*., "Determination of the Gate Breakdown Mechanisms in p-GaN Gate HEMTs by Multiple-Gate-Sweep Measurements," *IEEE Trans. Electron Devices,* vol. 68, no. 4, pp. 1518-1523, Jan. 2021, doi: 10.1109/ted.2021.3057007.

[3] B. Shankar, A. Soni, H. Chandrasekar, S. Raghavan, and M. Shrivastava, "First observations on the trap-induced avalanche instability and safe operating area concerns in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3433-3440, Jun. 2019, doi: 10.1109/ted.2019.2919491.

[4] L. Zhang, Z. Zheng, S. Yang, W. Song, J. He, and K. J. Chen, "p-GaN Gate HEMT with Surface Reinforcement for Enhanced Gate Reliability," *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 22-25, Jan. 2021, doi: 10.1109/led.2020.3037186.

[5] M. Ge *et al.*, "Gate Reliability of p-GaN Gate AlGaN/GaN High Electron Mobility Transistors," *IEEE Electron Device Lett.,* vol. 40, no. 3, pp. 379-382, Mar. 2019, doi: 10.1109/led.2019.2893290.

[6] N. E. Posthuma *et al*., "An Industry-Ready 200 mm p-GaN E-mode GaN-on-Si power Technology," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, May 2018, pp. 284-287, doi: 10.1109/ISPSD.2018.8393658.

[7] B. Shankar, A. Soni, S. Raghavan, and M. Shrivastava, "Trap-Assisted and Stress Induced Safe Operating Area Limits of AlGaN/GaN HEMTs," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 4, pp. 767-774, Oct. 2020, doi: 10.1109/tdmr.2020.3033522.

[8] Z. Jiang, L. Li, C. Wang, J. Zhao, and M. Hua, "Gate-Bias Induced Threshold Voltage (VTH) Instability in P-N Junction/AlGaN/GaN HEMT," *IEEE Trans. Electron Devices*, pp. 1-6, Jul. 2022, doi: 10.1109/ted.2022.3177397.

[9] N. E. Posthuma *et al.*, "Impact of Mg out-diffusion and activation on the p-GaN gate HEMT device performance," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, Jun. 2016, pp. 95-98, doi: 10.1109/ISPSD.2016.7520786.

[10] J. He, G. Tang, and K. J. Chen, "V_{TH} Instability of p-GaN Gate HEMTs under Static and Dynamic Gate Stress," *IEEE Electron Device Lett.,* vol. 39, no. 10, pp. 1576-1579, Aug. 2018, doi: 10.1109/led.2018.2867938.

[11] X. Li *et al*., "Observation of Dynamic V_{TH} of p-GaN Gate HEMTs by Fast Sweeping Characterization," *IEEE Electron Device Lett.,* vol. 41, no. 4, pp. 577-580, Feb. 2020, doi: 10.1109/led.2020.2972971.

[12] S. Li *et al*., "Comparison Investigations on Unclamped-Inductive-Switching Behaviors of Power GaN Switching Devices," *IEEE Trans. on Industrial Electron.,* vol. 69, no. 5, pp. 5041-5049, May 2021, doi: 10.1109/tie.2021.3076705.

[13] T.-L. Wu *et al.,* "Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001-1003, Oct. 2015, doi: 10.1109/led.2015.2465137.

[14] L. Zhang *et al.*, "AlGaN-Channel Gate Injection Transistor on Silicon Substrate With Adjustable 4–7-V Threshold Voltage and 1.3-kV Breakdown Voltage," *IEEE Electron Device Lett.,* vol. 39, no. 7, pp. 1026-1029, May 2018, doi: 10.1109/led.2018.2838542.

[15] F. Zhou *et al*., "1.2 kV/25 A Normally off P-N Junction/AlGaN/GaN HEMTs With Nanosecond Switching Characteristics and Robust Overvoltage Capability," *IEEE Trans. Power Electron.,* vol. 37, no. 1, pp. 26-30, Jan. 2022, doi: 10.1109/tpel.2021.3095937.

[16] A. Soni, K. M. Amogh, and M. Shrivastava, "Design Guidelines and Performance Tradeoffs in Recessed AlGaN/GaN Schottky Barrier Diodes," *IEEE Trans. Electron Devices,* vol. 67, no. 11, pp. 4834-4841, Nov. 2020, doi: 10.1109/ted.2020.3024354.

[17] X. Tang *et al*., "Demonstration of Electron/Hole Injections in the Gate of p-GaN/AlGaN/GaN Power Transistors and Their Effect on Device Dynamic Performance," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, May 2019, pp. 415-418.

[18] W. Yang and J.-S. Yuan, "Negative-Bias Temperature Instability of p-GaN Gate GaN-on-Si Power Devices," *IEEE Trans. on Device and Materials Reliability*, vol. 22, no. 2, pp. 217-222, Mar. 2022, doi: 10.1109/tdmr.2022.3160396.

[19] A. N. Tallarico *et al*., "PBTI in GaN-HEMTs With p-Type Gate: Role of the Aluminum Content on VTH and Underlying Degradation Mechanisms," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 38-44, Jan. 2018, doi: 10.1109/ted.2017.2769167.

[20] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True Breakdown Voltage and Overvoltage Margin of GaN Power HEMTs in Hard Switching," *IEEE Electron Device Lett.,* vol. 42, no. 4, pp. 505-508, Mar. 2021, doi: 10.1109/led.2021.3063360.

[21] A. N. Tallarico, S. Stoffels, N. Posthuma, S. Decoutere, E. Sangiorgi, and C. Fiegna, "Threshold Voltage Instability in GaN HEMTs With p-Type Gate: Mg Doping Compensation," *IEEE Electron Device Lett.,* vol. 40, no. 4, pp. 518-521, Apr. 2019, doi: 10.1109/led.2019.2897911.

[22] Z. Wang *et al.*, "Majority and Minority Carrier Traps in NiO/β -Ga_2O_3 p^+-n Heterojunction Diode," *IEEE Trans. Electron Devices,* pp. 1-7, Jan. 2022, doi: 10.1109/ted.2022.3143491.

[23] S. Yang *et al.*, "Identification of Trap States in p-GaN Layer of a p-GaN/AlGaN/GaN Power HEMT Structure by Deep-Level Transient Spectroscopy," *IEEE Electron Device Lett.,* vol. 41, no. 5, pp. 685-688, May 2020, doi: 10.1109/led.2020.2980150.

[24] S. Zeng *et al.*, "Origin of the red luminescence in Mg-doped GaN," *Appl. Phys. Lett*., vol. 89, no. 2, Jul. Jul. 2006, Art no. 022107, doi: 10.1063/1.2220552.

[25] Q. Yan, A. Janotti, M. Scheffler, and C. G. Van de Walle, "Role of nitrogen vacancies in the luminescence of Mg-doped GaN," *Appl. Phys. Lett.,* vol. 100, no. 14, Apr. 2012, doi: 10.1063/1.3699009.

[26] J. T. Chen, M. Y. Hua, J. L. Jiang, J. B. He, J. Wei, and K. J. Chen, "Impact of Hole-Deficiency and Charge Trapping on Threshold Voltage Stability of p-GaN HEMT under Reverse-bias Stress," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, Sep. 2020.