CE65H270DNCI

CoreGaN 650V GaN HEMT

Description

The CE65H270DNCI Series 650V, 270mΩ gallium nitride (GaN) FETs are normally-off devices.

Corenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Corenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

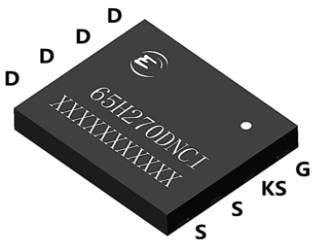
Easy to drive—compatible with standard gate drivers

Low conduction and switching losses

RoHS compliant and Halogen-free

Ordering Information

Part Number	Package	Package Configuration
CE65H270DNCI	DFN 5*6	Source



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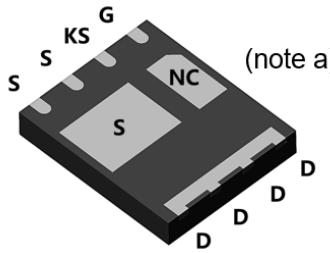
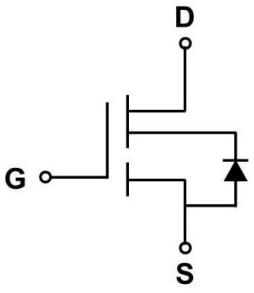


bottom

Note :

a. NC solder pad represents GaN source & MOS Drain; The electrical connection is prohibited.



Circuit Symbol

Benefits

Increased efficiency through fast switching

Increased power density

Reduced system size and weight

Features

BV_{DSS}	R_{DSON}	I_{DS}	Q_G
650V	270mΩ	9.3A	8.7nC

CorEnergy®

CE65H270DNCI

Absolute Maximum Ratings

T_c=25°C unless otherwise stated

Symbol	Parameter		Limit value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Drain to source voltage-transient [a]		800	
V_{GSS}	Gate to source voltage		-20~+20	
I_D	Continuous drain current @T_C=25°C [b]		9.3	A
	Continuous drain current @T_C=125°C [b]		4.2	
I_{DM}	Pulse drain current (pulse width: 10μs)		15	A
P_D	Maximum power dissipation @ T_C=25°C		56	W
T_C	Operating temperature	Case	-55~150	°C
T_J		Junction	-55~150	°C
T_S	Storage temperature		-55~150	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <1μs

b. For increased stability at high current operation

Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	2.2	°C /W

CE65H270DNCI

Electrical Parameters

T_j=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	V_{GS}= 0V
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	V_{DS}=1V, I_{DS}=1mA
$\triangle V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/°C	
$R_{DS(on)}$	Drain-source on-Resistance	-	270	320	mΩ	V_{GS}=10V, I_D=3A, T_J=25°C
		-	570	-		V_{GS}=10V, I_D=3A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	V_{DS}=650V, V_{GS}= 0V, T_J=25°C
		-	5	100		V_{DS}=650V, V_{GS}= 0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	-	-	±100	nA	V_{GS}=±20V
C_{ISS}	Input capacitance	-	333	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{OSS}	Output capacitance	-	18	-		
C_{RSS}	Reverse capacitance	-	3.7	-		
Q_G	Total gate charge	-	8.7	-	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=1A
Q_{GS}	Gate-source charge	-	2.2	-		
Q_{GD}	Gate-drain charge	-	2.6	-		
Q_{OSS}	Output charge	-	24	-	nC	V_{GS}=0V, V_{DS}=0V to 400V, f=1MHz
$t_{D(on)}$	Turn-on delay	-	5.9	-	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A, $R_{G-on(ext)}$=6.8Ω, $R_{G-off(ext)}$=2.2Ω, L=250μH
t_R	Rise time	-	3.4	-		
$t_{D(off)}$	Turn-off delay	-	12.5	-		
t_F	Fall time	-	14.9	-		

Electrical Parameters

T_j=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V_{SD}	Source-Drain reverse voltage	-	2.5	-	V	V_{GS}=0V, I_S=5A
t_{RR}	Reverse recovery time	-	14	-	ns	I_s=5A, V_{DD}=400V, di/dt=165A/μs
Q_{RR}	Reverse recovery charge	-	6.5	-	nC	

Typical Characteristics

T_j=25°C unless otherwise stated

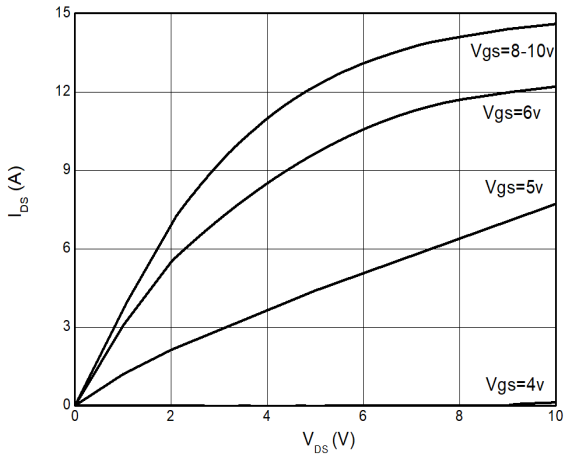


Figure 1. Typical Output Characteristics T_j=25°C

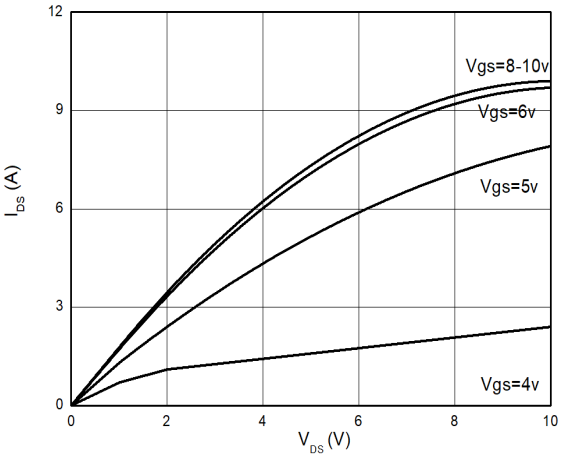


Figure 2. Typical Output Characteristics T_j=125°C

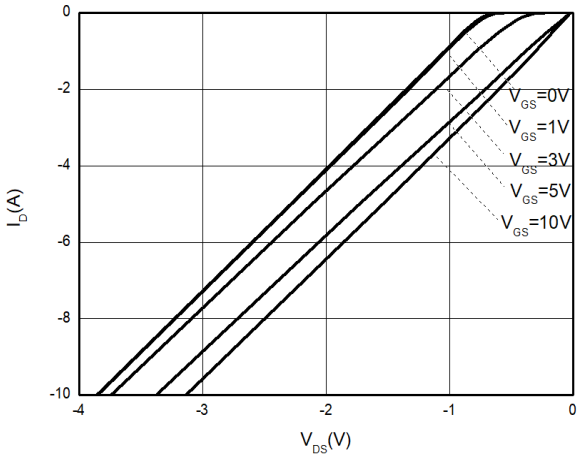


Figure 3. Channel Reverse Characteristics T_j=25°C

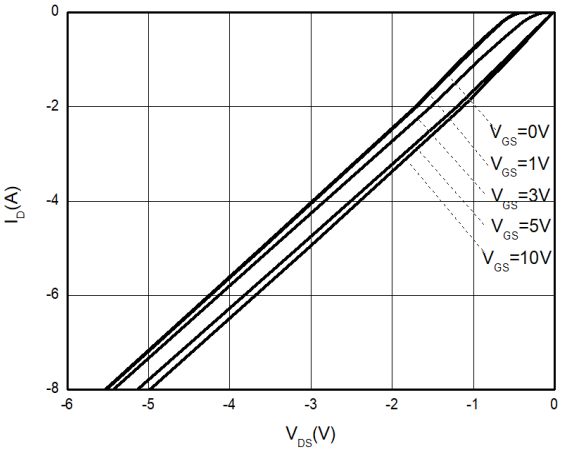


Figure 4. Channel Reverse Characteristics T_j=125°C

Typical Characteristics

T_j=25°C unless otherwise stated

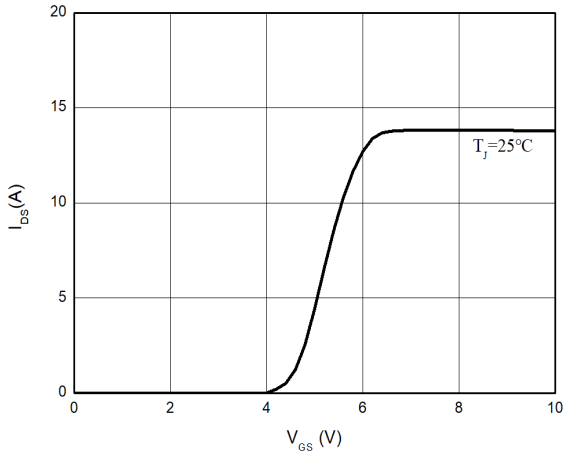


Figure 5. Typical Transfer Characteristics (V_{DS}=10V)

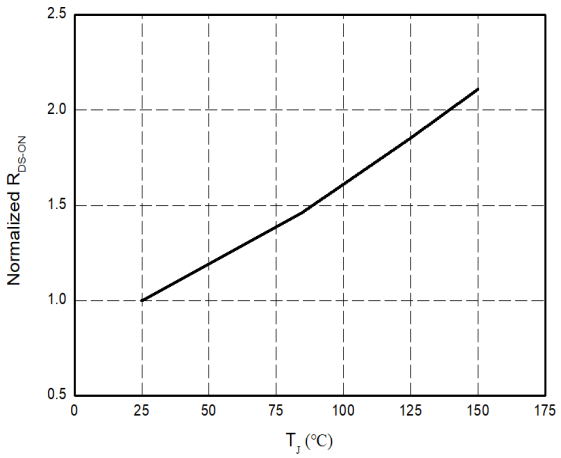


Figure 6. Normalized On-resistance

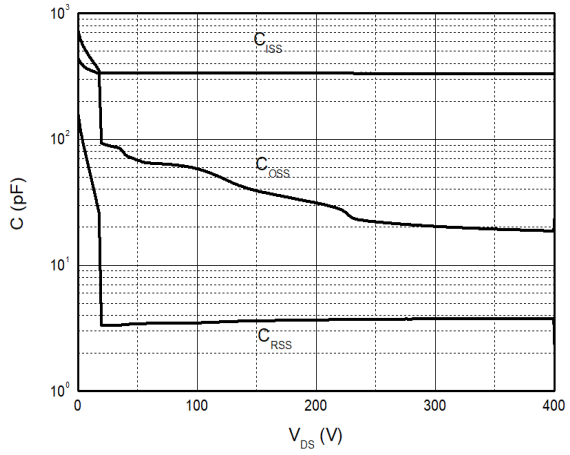


Figure 7. Typical Capacitance (f=1MHz)

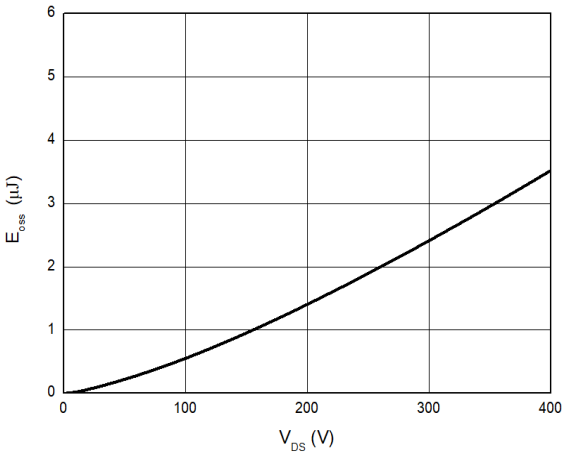


Figure 8. Typical C_{OSS} Stored Energy

Typical Characteristics

T_J=25°C unless otherwise stated

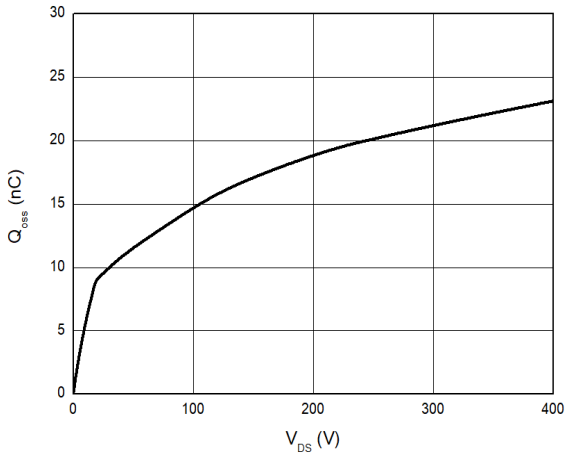


Figure 9. Typical Q_{OSS}

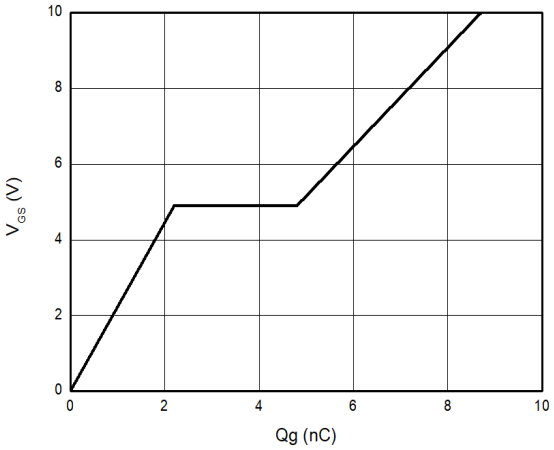


Figure 10. Typical Gate Charge (V_{DS}=400V, I_D=1A)

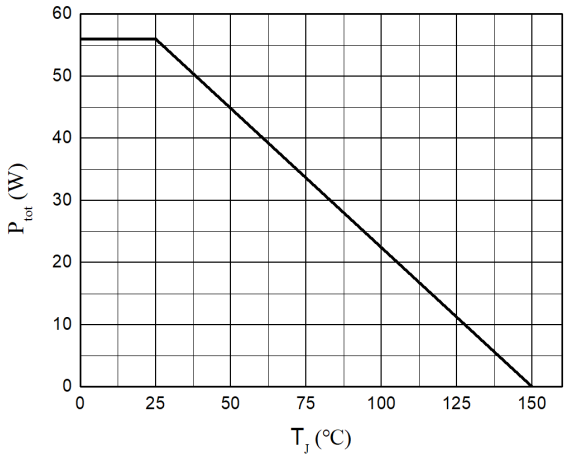


Figure 11. Power Dissipation

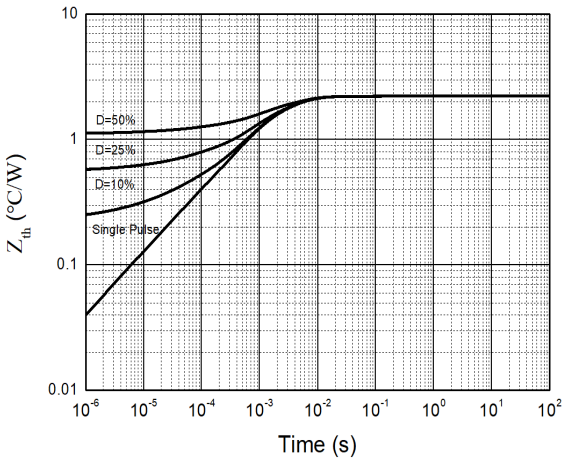


Figure 12. Transient Thermal Resistance

Typical Characteristics

T_J=25°C unless otherwise stated

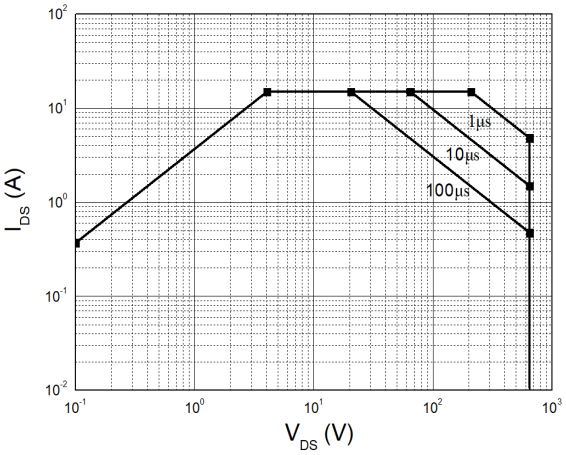


Figure 13. Safe Operating Area T_J=25°C

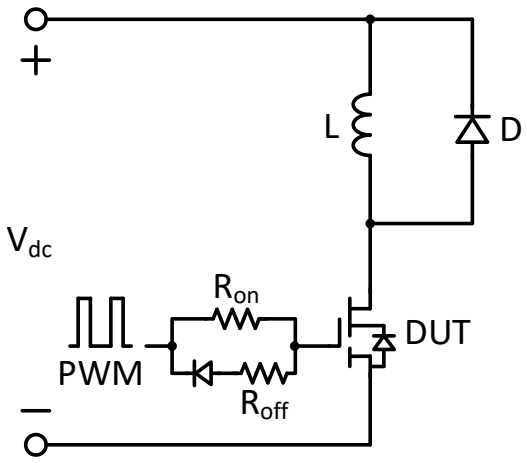


Figure 14. Switching times with inductive load

V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A, $R_{G\text{-}on(ext)}$=6.8Ω, $R_{G\text{-}off(ext)}$=2.2Ω, L=250µH

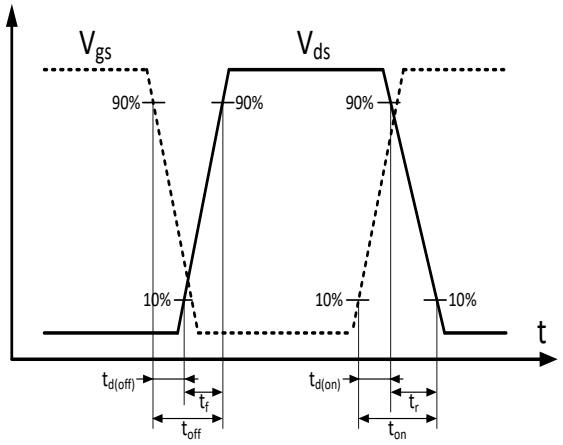
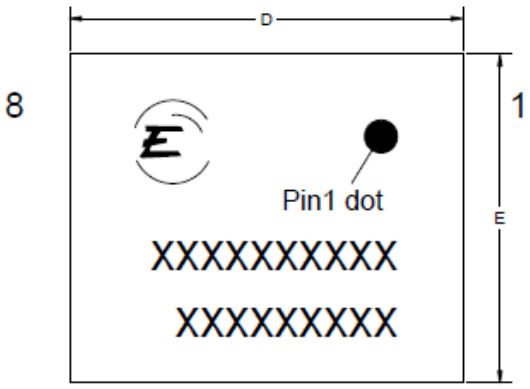


Figure 15. Switching times with waveform

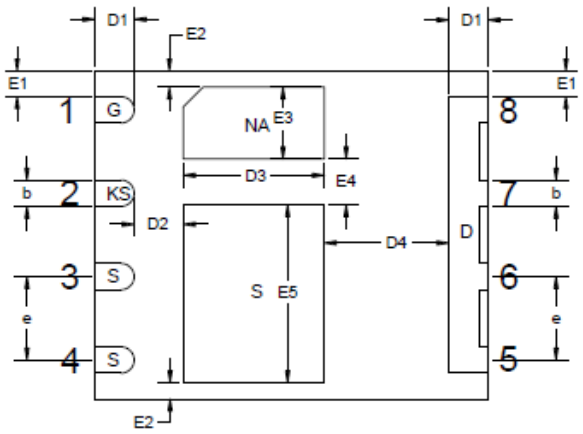
CE65H270DNCI

PACKAGE DIMENSIONS

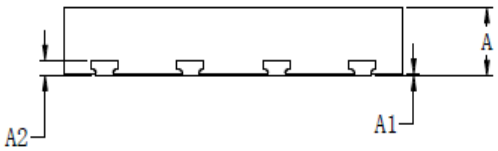
TOP VIEW



BOTTOM VIEW



Side View(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	0.850	0.900	0.950
A1	0.000	0.020	0.050
A2		0.203REF	
D	5.900	6.000	6.100
E	4.900	5.000	5.100
D1	0.500	0.600	0.700
D2	0.650	0.750	0.850
D3	2.050	2.150	2.250
D4	1.800	1.900	2.000
E1	0.295	0.395	0.495
E2	0.195	0.295	0.395
E3	0.990	1.090	1.190
E4	0.600	0.700	0.800
E5	2.610	2.710	2.810
b	0.300	0.400	0.500
e	1.170	1.270	1.370

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-12-25	Initial release
2.0	2025-01-02	Optimize application platform testing