



CoreGaN 650V GaN HEMT

Description

The CE65H270DNDI Series 650V, 270mΩ gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

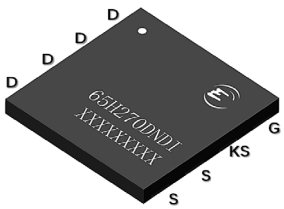
Easy to drive—compatible with standard gate drivers
Low conduction and switching losses
RoHS compliant and Halogen-free

Benefits

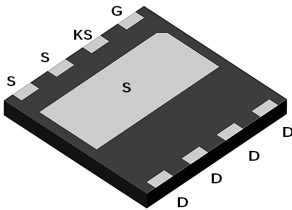
Increased efficiency through fast switching
Increased power density
Reduced system size and weight

Ordering Information

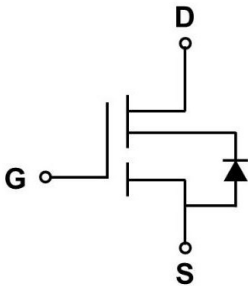
Part Number	Package	Package Configuration
CE65H270DNDI	DFN 8*8	Source



Top



Bottom



Circuit Symbol

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
650V	270mΩ	10.4A	8.8nC



Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$ unless otherwise stated

Symbol	Parameter		Limit value	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^{\circ}\text{C}$ to 150°C)		650	V
$V_{(TR)DSS}$	Drain to source voltage-transient ^a		800	
V_{GSS}	Gate to source voltage		-20 ~ +20	
I_D	Continuous drain current @ $T_C=25^{\circ}\text{C}$ ^b		10.4	A
	Continuous drain current @ $T_C=125^{\circ}\text{C}$ ^b		4.6	
I_{DM}	Pulse drain current (pulse width: 10 μs)		14.5	A
P_D	Maximum power dissipation @ $T_C=25^{\circ}\text{C}$		69	W
T_C	Operating temperature	Case	-55 ~ 150	$^{\circ}\text{C}$
T_J		Junction	-55 ~ 150	$^{\circ}\text{C}$
T_S	Storage temperature		-55 ~ 150	$^{\circ}\text{C}$

a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$

b. For increased stability at high current operation



CE65H270DNDI

Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	1.8	°C /W



Electrical Parameters

$T_J=25^{\circ}\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS}=0\text{V}$
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	$V_{DS}=1\text{V}, I_{DS}=1\text{mA}$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/ $^{\circ}\text{C}$	
$R_{DS(on)}$	Drain-source on-Resistance	-	270	320	m Ω	$V_{GS}=10\text{V}, I_D=3\text{A}, T_J=25^{\circ}\text{C}$
		-	570	-		$V_{GS}=10\text{V}, I_D=3\text{A}, T_J=150^{\circ}\text{C}$
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_J=25^{\circ}\text{C}$
		-	5	100		$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_J=150^{\circ}\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$
C_{ISS}	Input capacitance	-	330	-	pF	$V_{GS}=0\text{V}, V_{DS}=400\text{V}, f=1\text{MHz}$
C_{OSS}	Output capacitance	-	15	-		
C_{RSS}	Reverse capacitance	-	1.1	-		
Q_G	Total gate charge	-	8.7	-	nC	$V_{DS}=400\text{V}, V_{GS}=0\text{V to }10\text{V}, I_D=1\text{A}$
Q_{GS}	Gate-source charge	-	2.2	-		
Q_{GD}	Gate-drain charge	-	2.6	-		
Q_{OSS}	Output charge	-	22	-	nC	$V_{GS}=0\text{V}, V_{DS}=0\text{V to }400\text{V}, f=1\text{MHz}$
$t_{D(on)}$	Turn-on delay	-	5.9	-	ns	$V_{DS}=400\text{V}, V_{GS}=0\text{V to }10\text{V}, I_D=2.1\text{A},$ $R_{G-on(ext)}=6.8\Omega, R_{G-off(ext)}=2.2\Omega,$ $L=250\mu\text{H}$
t_R	Rise time	-	3.4	-		
$t_{D(off)}$	Turn-off delay	-	12.5	-		
t_F	Fall time	-	14.9	-		



Electrical Parameters

T_J=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V _{SD}	Source-Drain reverse voltage	-	2.3	-	V	V _{GS} =0V, I _S =5A
t _{RR}	Reverse recovery time	-	14	-	ns	I _S =5A, V _{DD} =400V, di/dt=165A/μs
Q _{RR}	Reverse recovery charge	-	6.5	-	nC	



Typical Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise stated

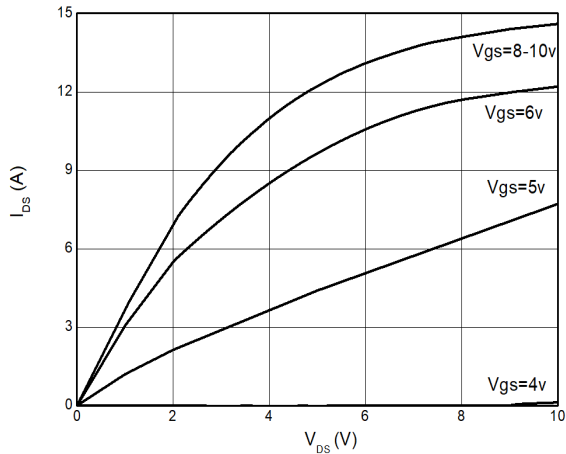


Figure 1. Typical Output Characteristics $T_J = 25^\circ\text{C}$

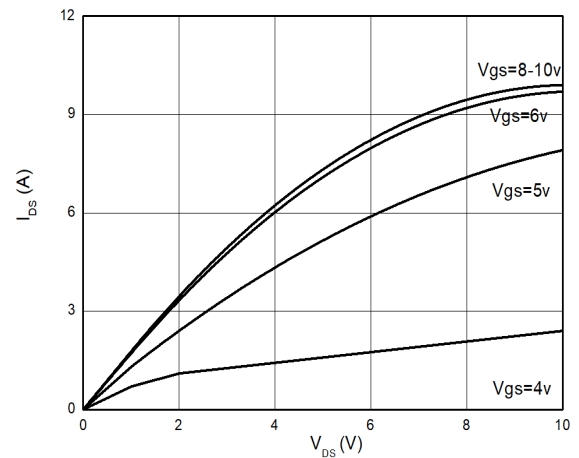


Figure 2. Typical Output Characteristics $T_J = 125^\circ\text{C}$

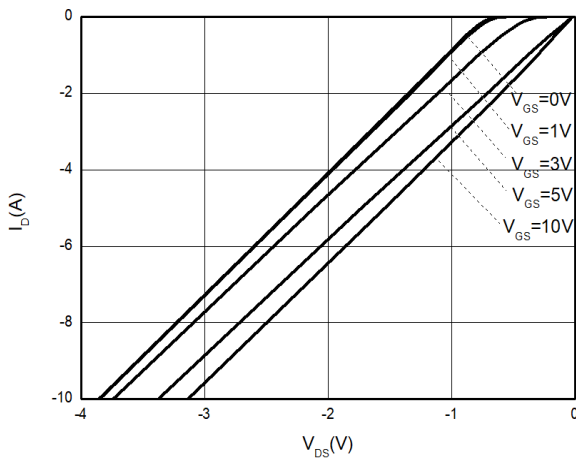


Figure 3. Channel Reverse Characteristics $T_J = 25^\circ\text{C}$

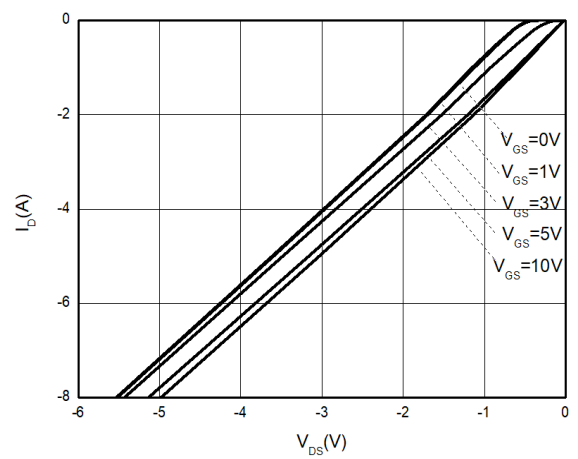


Figure 4. Channel Reverse Characteristics $T_J = 125^\circ\text{C}$



Typical Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise stated

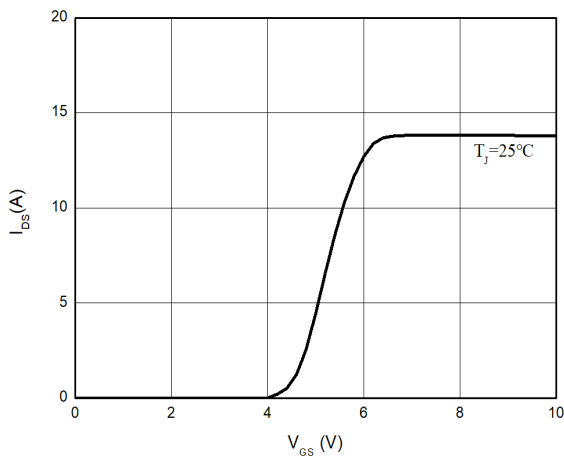


Figure 5. Typical Transfer Characteristics ($V_{DS}=10V$)

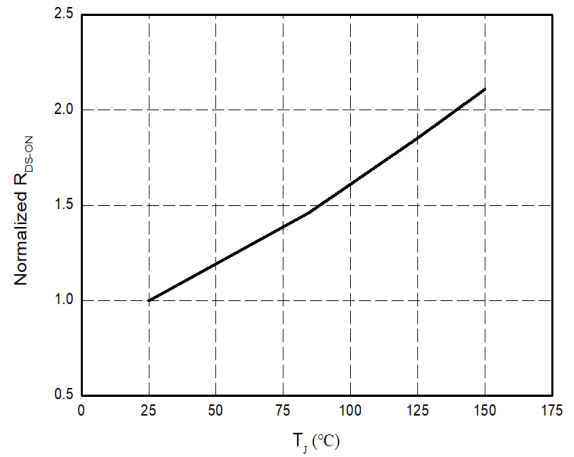


Figure 6. Normalized On-resistance

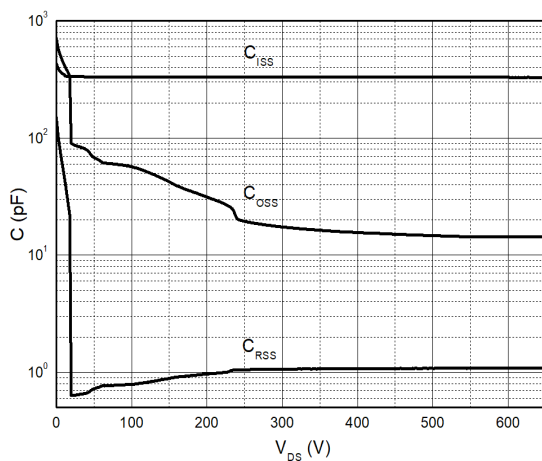


Figure 7. Typical Capacitance ($f=1\text{MHz}$)

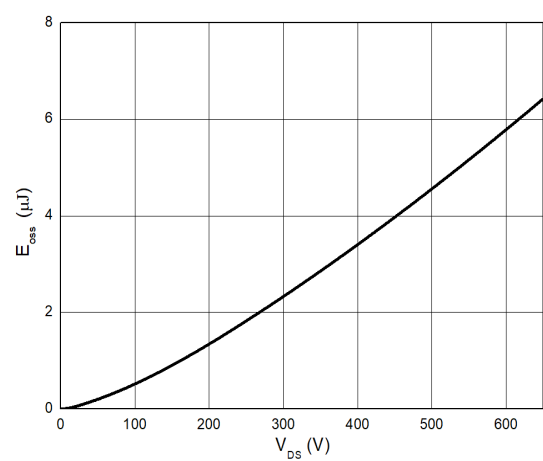


Figure 8. Typical C_{OSS} Stored Energy



Typical Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise stated

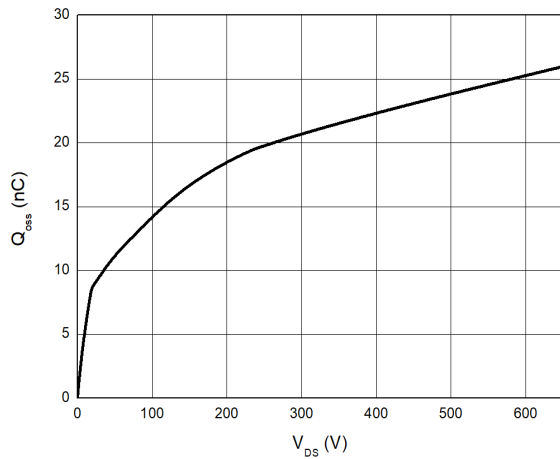


Figure 9. Typical Q_{oss}

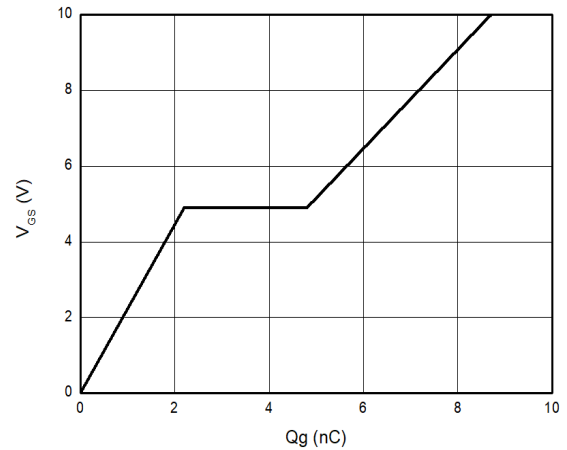


Figure 10. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)

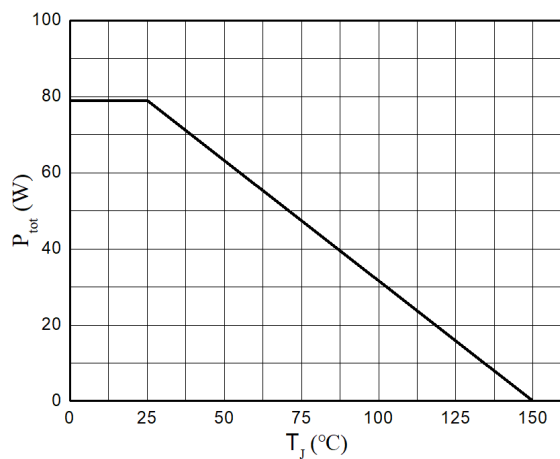


Figure 11. Power Dissipation

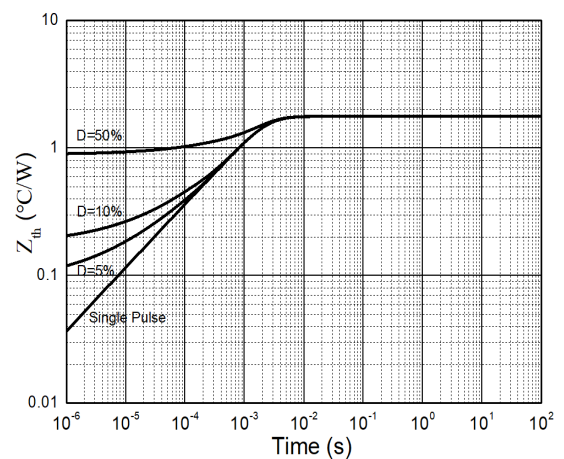


Figure 12. Transient Thermal Resistance



Typical Characteristics

$T_J=25^\circ\text{C}$ unless otherwise stated

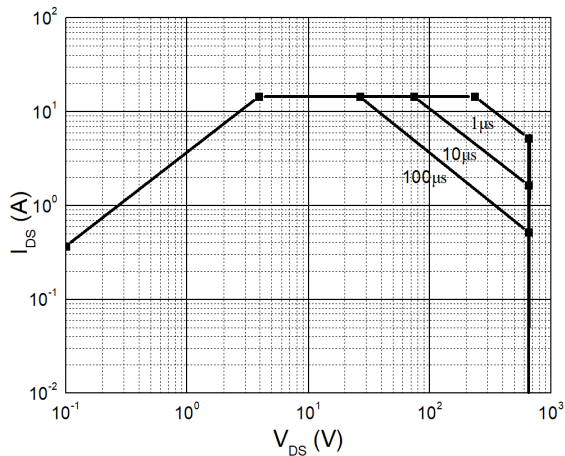


Figure 13. Safe Operating Area $T_c=25^\circ\text{C}$

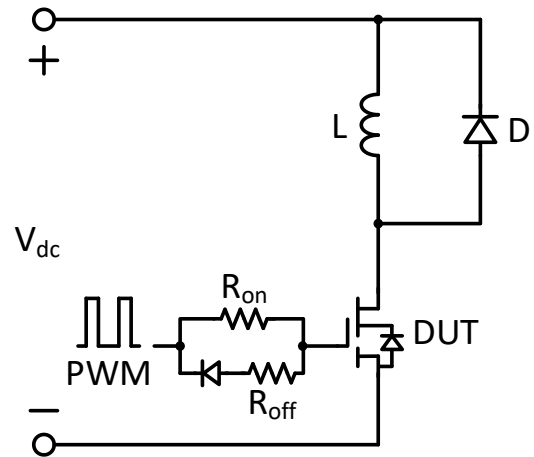


Figure 14. Switching times with inductive load

$V_{DS}=400\text{V}$, $V_{GS}=0\text{V to }10\text{V}$, $I_D=2.1\text{A}$,
 $R_{G-on(ext)}=6.8\Omega$, $R_{G-off(ext)}=2.2\Omega$, $L=250\mu\text{H}$

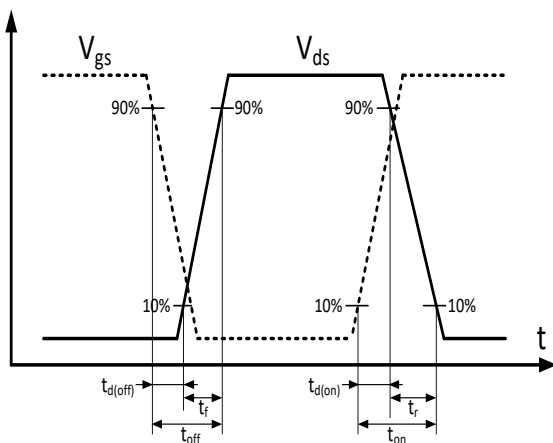


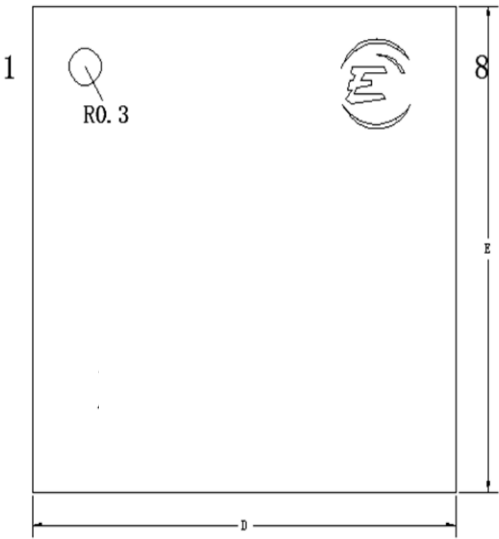
Figure 15. Switching times with waveform



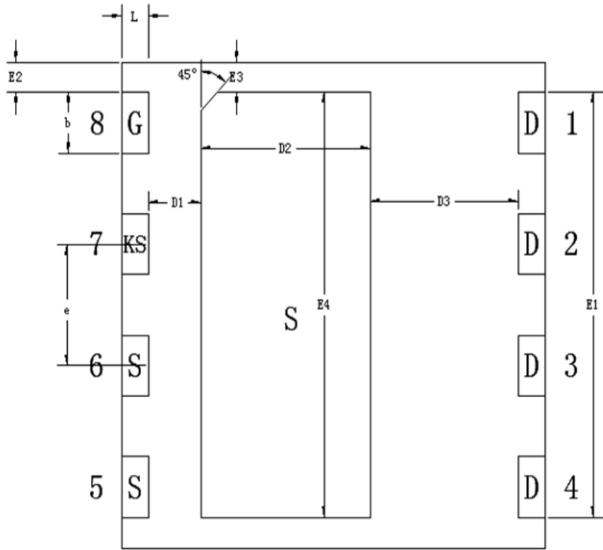
PACKAGE DIMENSIONS

DFN8x8-8L-1.10-A

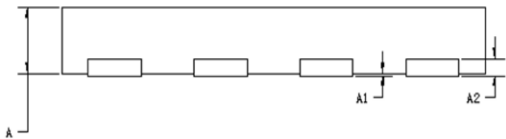
Top view



Bottom view



Side view(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	1.05	1.10	1.15
A1	0	0.02	0.05
A2	0.203REF		
D	7.9	8	8.1
E	7.9	8	8.1
D1	0.9	1	1.1
D2	3.1	3.2	3.3
D3	2.7	2.8	2.9
E1	6.9	7	7.1
E2	0.4	0.5	0.6
E3	0.4	0.5	0.6
E4	6.9	7	7.1
e	1.9	2	2.1
b	0.9	1	1.1
L	0.4	0.5	0.6



CE65H270DNDI

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-02-28	Initial release
2.0	2024-06-01	Enrich dynamic specification curves
3.0	2025-01-02	Optimize application platform testing