

**CE65H450DNCI**

CoreGaN 650V GaN HEMT

Description

The CE65H450DNCI Series 650V, 450mΩ gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

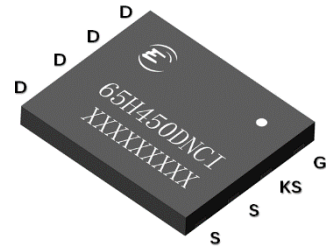
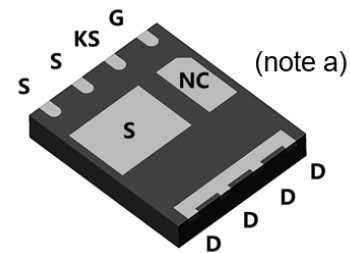
Easy to drive—compatible with standard gate drivers
Low conduction and switching losses
RoHS compliant and Halogen-free

Benefits

Increased efficiency through fast switching
Increased power density
Reduced system size and weight

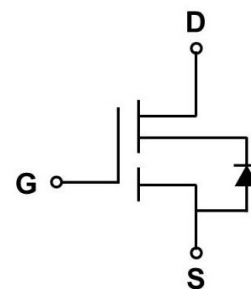
Ordering Information

Part Number	Package	Package Configuration
CE65H450DNCI	DFN 5*6	Source

**Top****Bottom**

Note :

- a. NC solder pad represents GaN source & MOS Drain;
The electrical connection is prohibited.



Circuit Symbol

Features

BV_{DSS}	$R_{DS(ON)}$	I_{DS}	Q_G
650V	450mΩ	6.5A	7.6nC



Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter		Limit value	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)		650	V
$V_{(TR)DSS}$	Drain to source voltage-transient ^a		800	
V_{GSS}	Gate to source voltage		-20 ~ +20	
I_D	Continuous drain current @ $T_c = 25^\circ\text{C}$ ^b		6.5	A
	Continuous drain current @ $T_c = 125^\circ\text{C}$ ^b		2.8	
I_{DM}	Pulse drain current (pulse width: 10 μs)		10.5	A
P_D	Maximum power dissipation @ $T_c = 25^\circ\text{C}$		43	W
T_c	Operating temperature	Case	-55 ~ 150	$^\circ\text{C}$
T_J		Junction	-55 ~ 150	$^\circ\text{C}$
T_S	Storage temperature		-55 ~ 150	$^\circ\text{C}$

a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$

b. For increased stability at high current operation



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Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	2.9	°C /W



Electrical Parameters

$T_J = 25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS} = 0V$
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	$V_{DS} = 1V, I_{DS} = 1mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Drain-source on-Resistance	-	450	520	m Ω	$V_{GS} = 10V, I_D = 2A, T_J = 25^\circ\text{C}$
		-	940	-		$V_{GS} = 10V, I_D = 2A, T_J = 150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	-	2	10	μA	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$
		-	5	100		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	± 100	nA	$V_{GS} = \pm 20V$
C_{ISS}	Input capacitance	-	335	-	pF	$V_{GS} = 0V, V_{DS} = 400V, f = 1MHz$
C_{OSS}	Output capacitance	-	11	-		
C_{RSS}	Reverse capacitance	-	0.9	-		
Q_G	Total gate charge	-	7.6	-	nC	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 1A$
Q_{GS}	Gate-source charge	-	2.3	-		
Q_{GD}	Gate-drain charge	-	2.8	-		
Q_{OSS}	Output charge	-	17	-	nC	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V, f = 1MHz$
$t_{D(on)}$	Turn-on delay	-	5.1	-	ns	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 2.1A, R_{G-on(ext)} = 6.8\Omega, R_{G-off(ext)} = 2.2\Omega, L = 250\mu H$
t_R	Rise time	-	3.6	-		
$t_{D(off)}$	Turn-off delay	-	10	-		
t_F	Fall time	-	12.6	-		



Electrical Parameters

T_j=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V _{SD}	Source-Drain reverse voltage	-	2.2	-	V	V _{GS} =0V, I _S =2.5A
t _{RR}	Reverse recovery time	-	14	-	ns	I _S =2.5A, V _{DD} =400V, di/dt=165A/μs
Q _{RR}	Reverse recovery charge	-	6.5	-	nC	



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

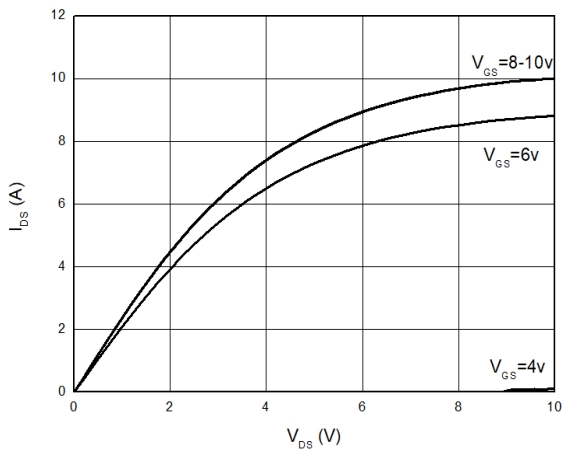


Figure 1. Typical Output Characteristics $T_j = 25^\circ\text{C}$

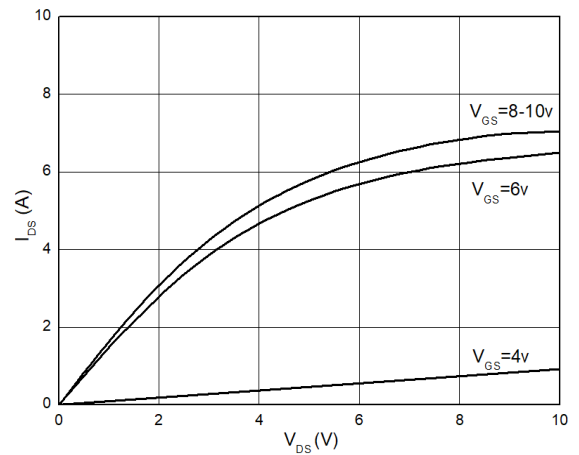


Figure 2. Typical Output Characteristics $T_j = 125^\circ\text{C}$

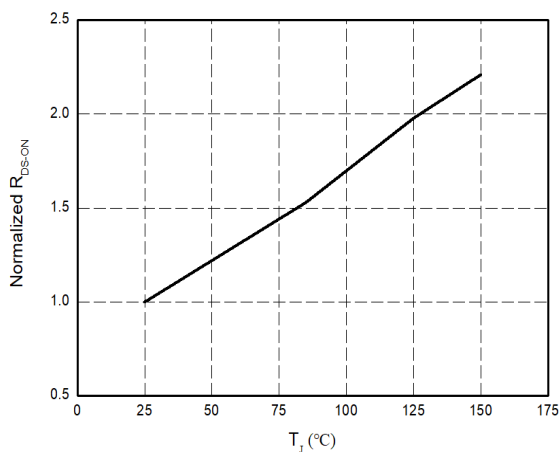


Figure 3. Normalized On-resistance

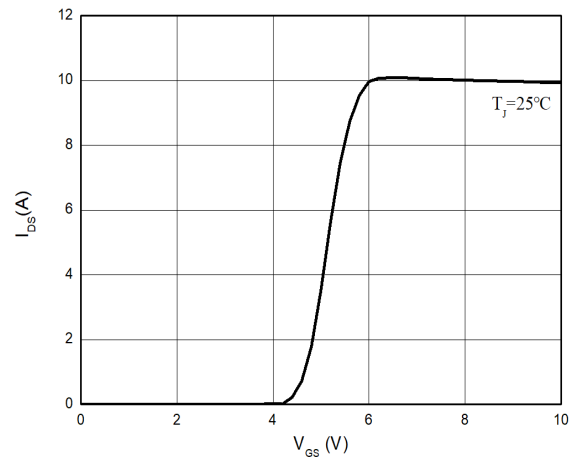


Figure 4. Typical Transfer Characteristics $T_j = 25^\circ\text{C}$



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Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

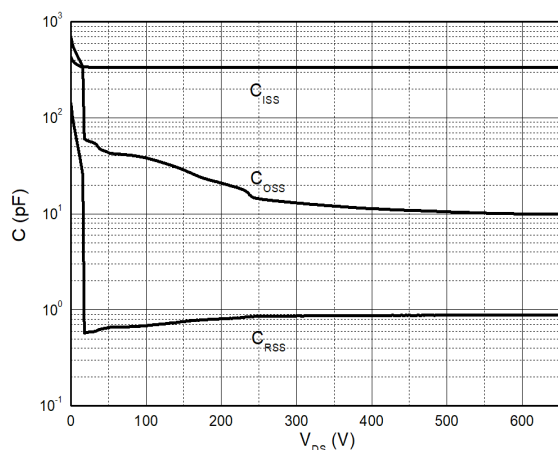


Figure 5. Typical Capacitance ($f=1\text{MHz}$)

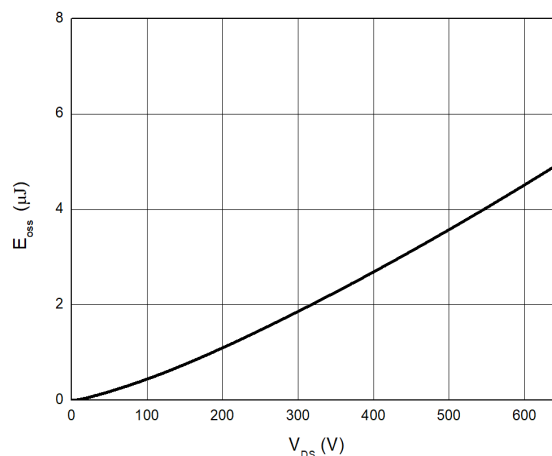


Figure 6. Typical C_{OSS} Stored Energy

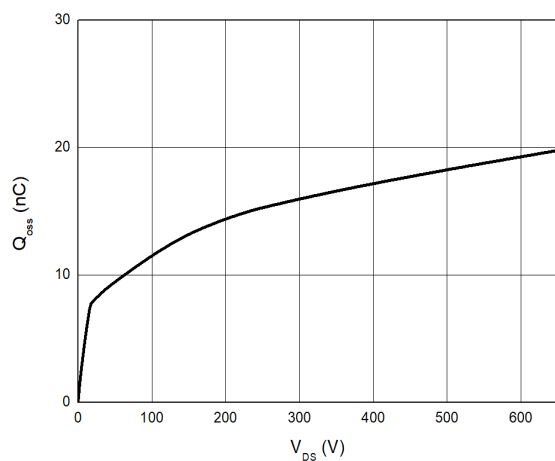


Figure 7. Typical Q_{OSS}

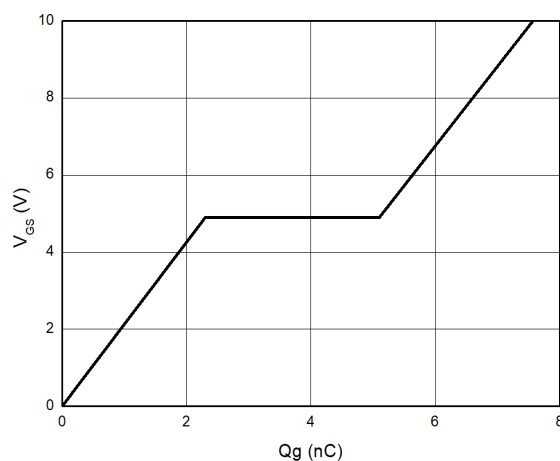


Figure 8. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

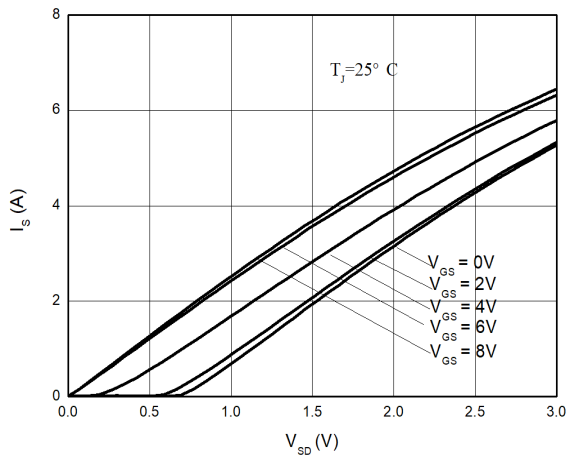


Figure 9. Channel Reverse Characteristics $T_j = 25^\circ\text{C}$

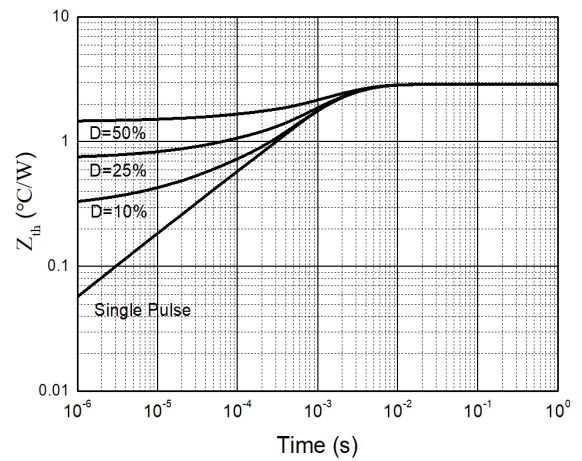


Figure 10. Transient Thermal Resistance

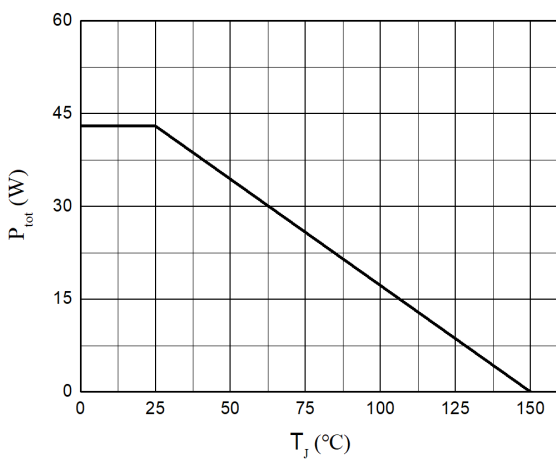


Figure 11. Power Dissipation

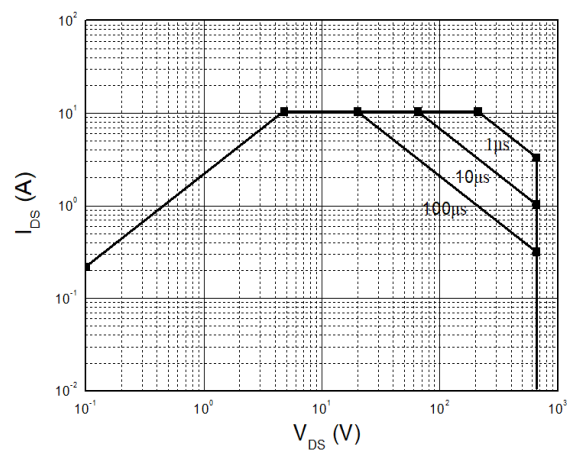


Figure 12. Safe Operating Area $T_j = 25^\circ\text{C}$

Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

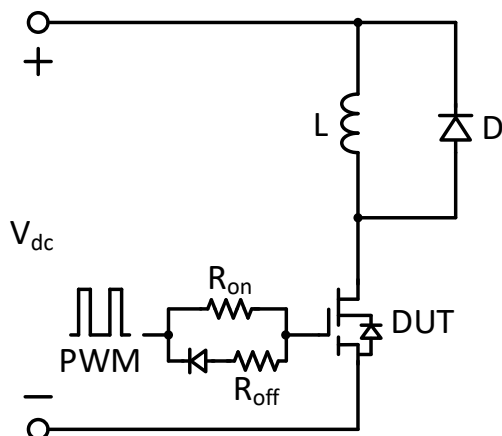


Figure 13. Switching times with inductive load

$V_{DS} = 400\text{V}$, $V_{GS} = 0\text{V to } 10\text{V}$, $I_D = 2.1\text{A}$,

$R_{G-on(ext)} = 6.8\Omega$, $R_{G-off(ext)} = 2.2\Omega$, $L = 250\mu\text{H}$

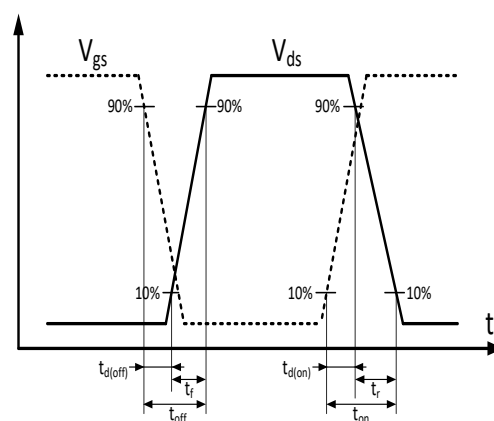
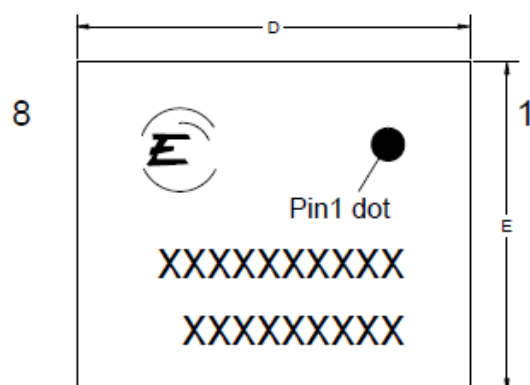


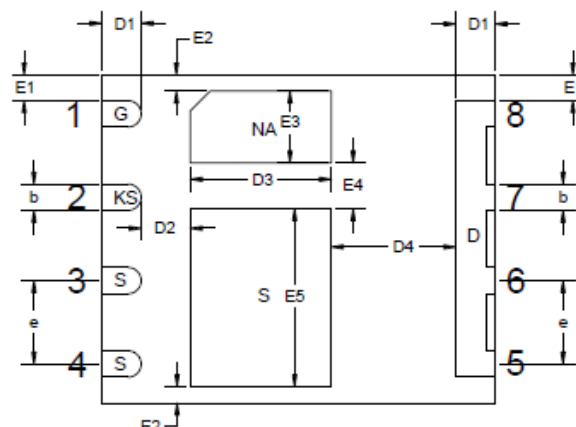
Figure 14. Switching times with waveform

PACKAGE DIMENSIONS

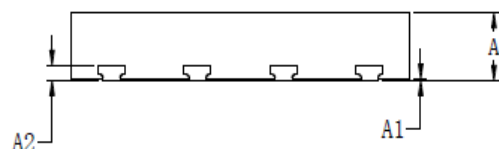
TOP VIEW



BOTTOM VIEW



Side View(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	0.850	0.900	0.950
A1	0.000	0.020	0.050
A2	0.203REF		
D	5.900	6.000	6.100
E	4.900	5.000	5.100
D1	0.500	0.600	0.700
D2	0.650	0.750	0.850
D3	2.050	2.150	2.250
D4	1.800	1.900	2.000
E1	0.295	0.395	0.495
E2	0.195	0.295	0.395
E3	0.990	1.090	1.190
E4	0.600	0.700	0.800
E5	2.610	2.710	2.810
b	0.300	0.400	0.500
e	1.170	1.270	1.370



CE65H450DNCI

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-05-06	Initial release
2.0	2025-01-02	Optimize application platform testing