

**CE65H450TOEI**

CoreGaN 650V GaN HEMT

Description

The CE65H450TOEI Series 650V, 450mΩ gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

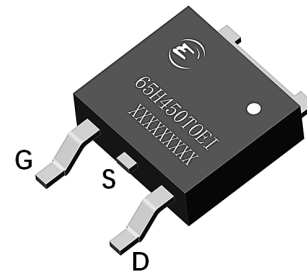
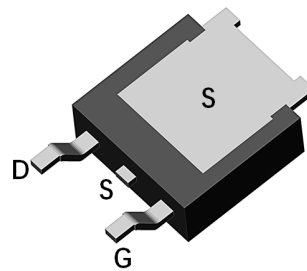
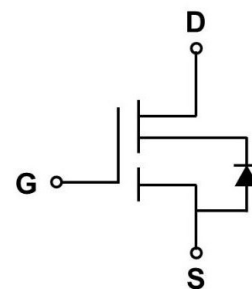
Easy to drive—compatible with standard gate drivers
 Low conduction and switching losses
 RoHS compliant and Halogen-free

Benefits

Increased efficiency through fast switching
 Increased power density
 Reduced system size and weight

Ordering Information

Part Number	Package	Package Configuration
CE65H450TOEI	TO252	Source

**Top****Bottom**

Circuit Symbol

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
650V	450mΩ	7A	7.6nC



Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter		Limit value	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)		650	V
$V_{(TR)DSS}$	Drain to source voltage-transient ^a		800	
V_{GSS}	Gate to source voltage		-20 ~ +20	
I_D	Continuous drain current @ $T_c = 25^\circ\text{C}$ ^b		7	A
	Continuous drain current @ $T_c = 125^\circ\text{C}$ ^b		3	
I_{DM}	Pulse drain current (pulse width: 10 μs)		10.5	A
P_D	Maximum power dissipation @ $T_c = 25^\circ\text{C}$		52	W
T_c	Operating temperature	Case	-55 ~ 150	$^\circ\text{C}$
T_J		Junction	-55 ~ 150	$^\circ\text{C}$
T_S	Storage temperature		-55 ~ 150	$^\circ\text{C}$

a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$

b. For increased stability at high current operation



Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	2.4	°C /W



Electrical Parameters

$T_J = 25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS} = 0V$
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	$V_{DS} = 1V, I_{DS} = 1mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Drain-source on-Resistance	-	450	520	m Ω	$V_{GS} = 10V, I_D = 2A, T_J = 25^\circ\text{C}$
		-	940	-		$V_{GS} = 10V, I_D = 2A, T_J = 150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	-	2	10	μA	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$
		-	5	100		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	± 100	nA	$V_{GS} = \pm 20V$
C_{ISS}	Input capacitance	-	335	-	pF	$V_{GS} = 0V, V_{DS} = 400V, f = 1MHz$
C_{OSS}	Output capacitance	-	11	-		
C_{RSS}	Reverse capacitance	-	0.9	-		
Q_G	Total gate charge	-	7.6	-	nC	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 1A$
Q_{GS}	Gate-source charge	-	2.3	-		
Q_{GD}	Gate-drain charge	-	2.8	-		
Q_{OSS}	Output charge	-	17	-	nC	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V, f = 1MHz$
$t_{D(on)}$	Turn-on delay	-	5.1	-	ns	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 2.1A, R_{G-on(ext)} = 6.8\Omega, R_{G-off(ext)} = 2.2\Omega, L = 250\mu H$
t_R	Rise time	-	3.6	-		
$t_{D(off)}$	Turn-off delay	-	10	-		
t_F	Fall time	-	12.6	-		



Electrical Parameters

T_j=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V _{SD}	Source-Drain reverse voltage	-	2.2	-	V	V _{GS} =0V, I _S =2.5A
t _{RR}	Reverse recovery time	-	14	-	ns	I _S =2.5A, V _{DD} =400V, di/dt=165A/μs
Q _{RR}	Reverse recovery charge	-	6.5	-	nC	



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

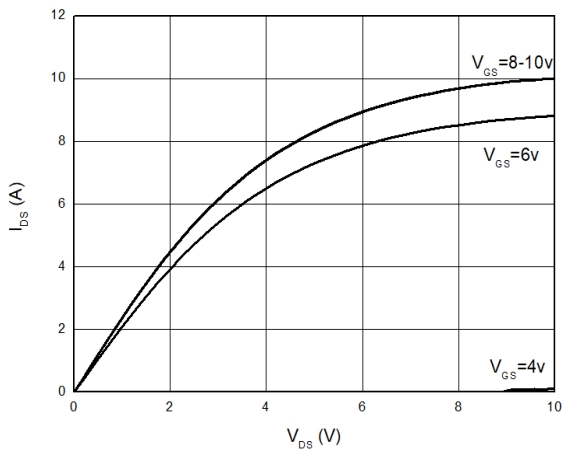


Figure 1. Typical Output Characteristics $T_j = 25^\circ\text{C}$

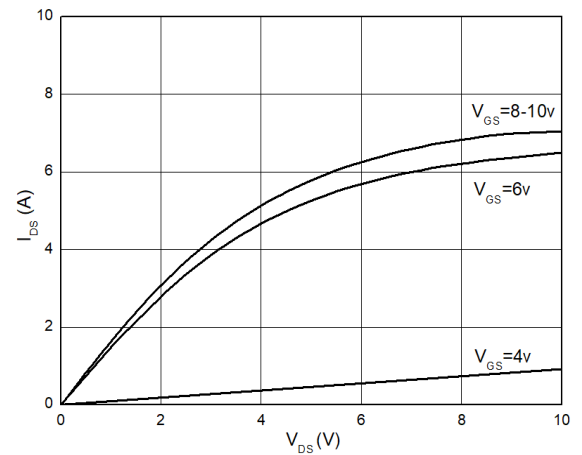


Figure 2. Typical Output Characteristics $T_j = 125^\circ\text{C}$

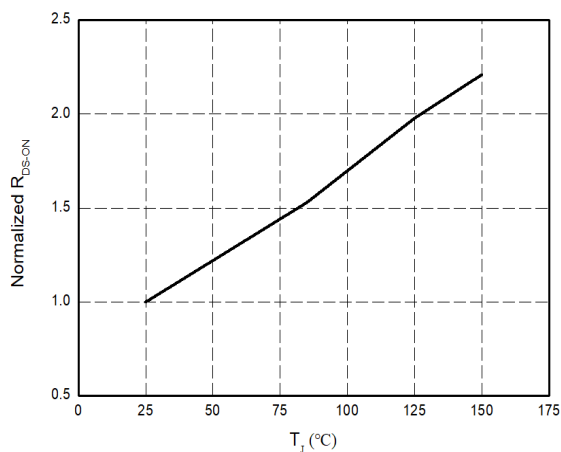


Figure 3. Normalized On-resistance

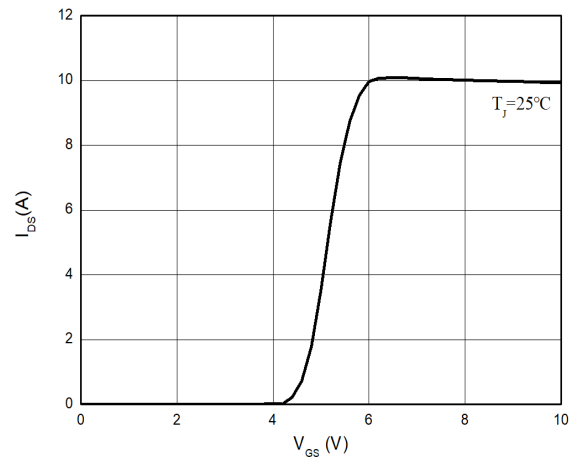


Figure 4. Typical Transfer Characteristics $T_j = 25^\circ\text{C}$



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

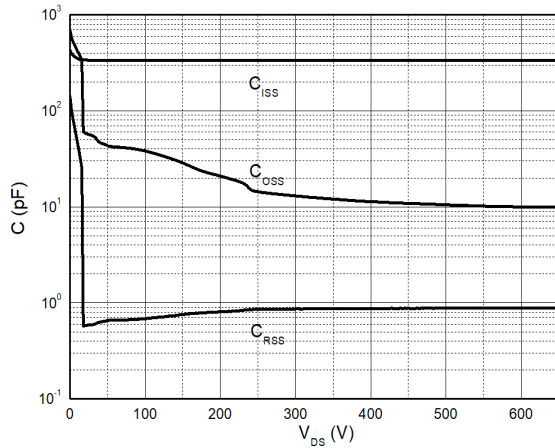


Figure 5. Typical Capacitance (f=1MHz)

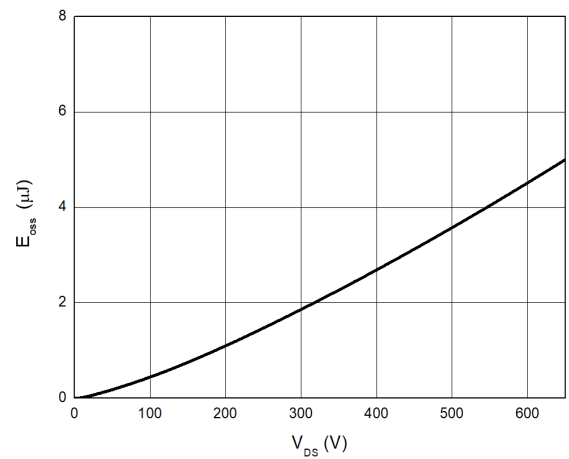


Figure 6. Typical C_{OSS} Stored Energy

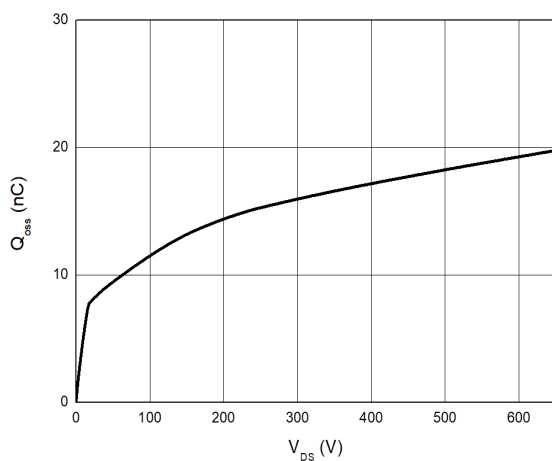


Figure 7. Typical Q_{OSS}

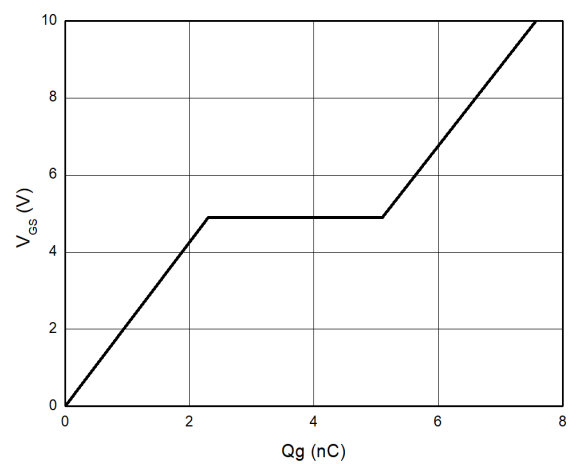


Figure 8. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

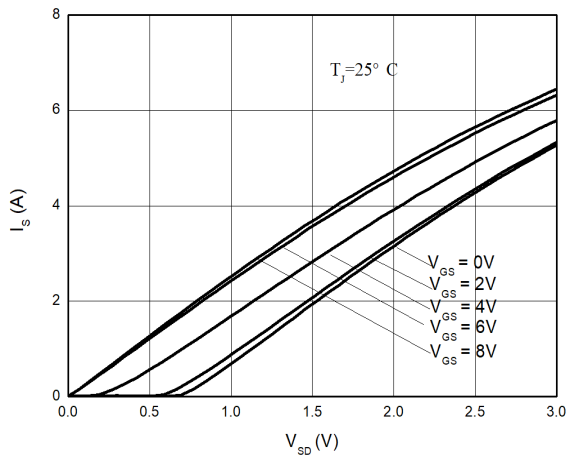


Figure 9. Channel Reverse Characteristics $T_j = 25^\circ\text{C}$

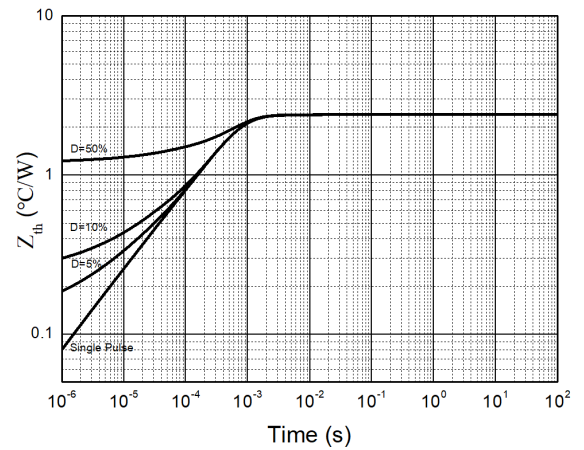


Figure 10. Transient Thermal Resistance

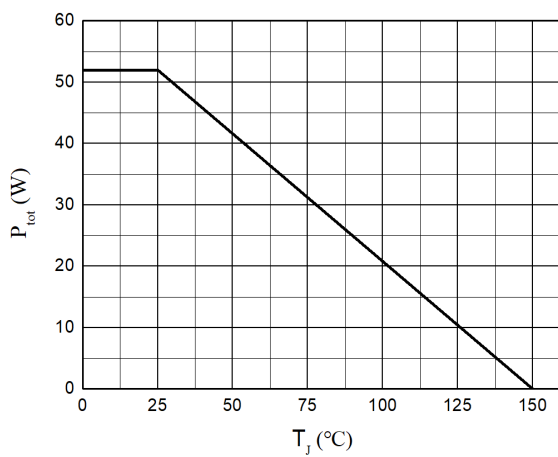


Figure 11. Power Dissipation

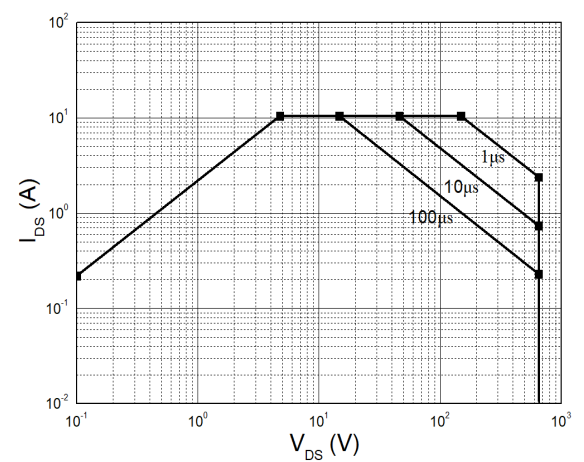


Figure 12. Safe Operating Area $T_j = 25^\circ\text{C}$



Typical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise stated

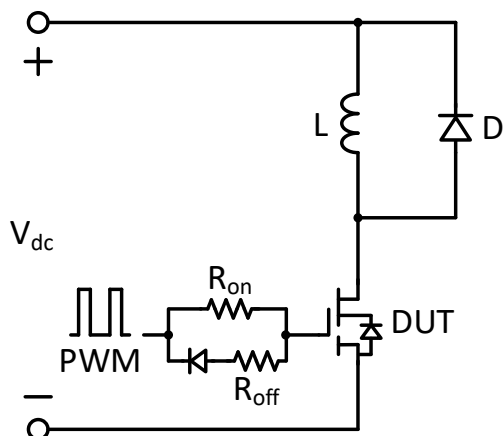


Figure 13. Switching times with inductive load

$V_{DS} = 400\text{V}$, $V_{GS} = 0\text{V to } 10\text{V}$, $I_D = 2.1\text{A}$,

$R_{G-on(ext)} = 6.8\Omega$, $R_{G-off(ext)} = 2.2\Omega$, $L = 250\mu\text{H}$

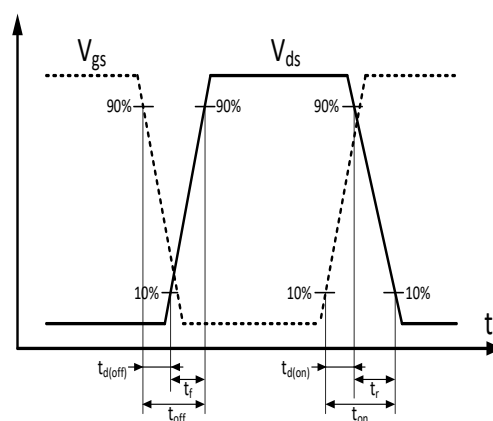
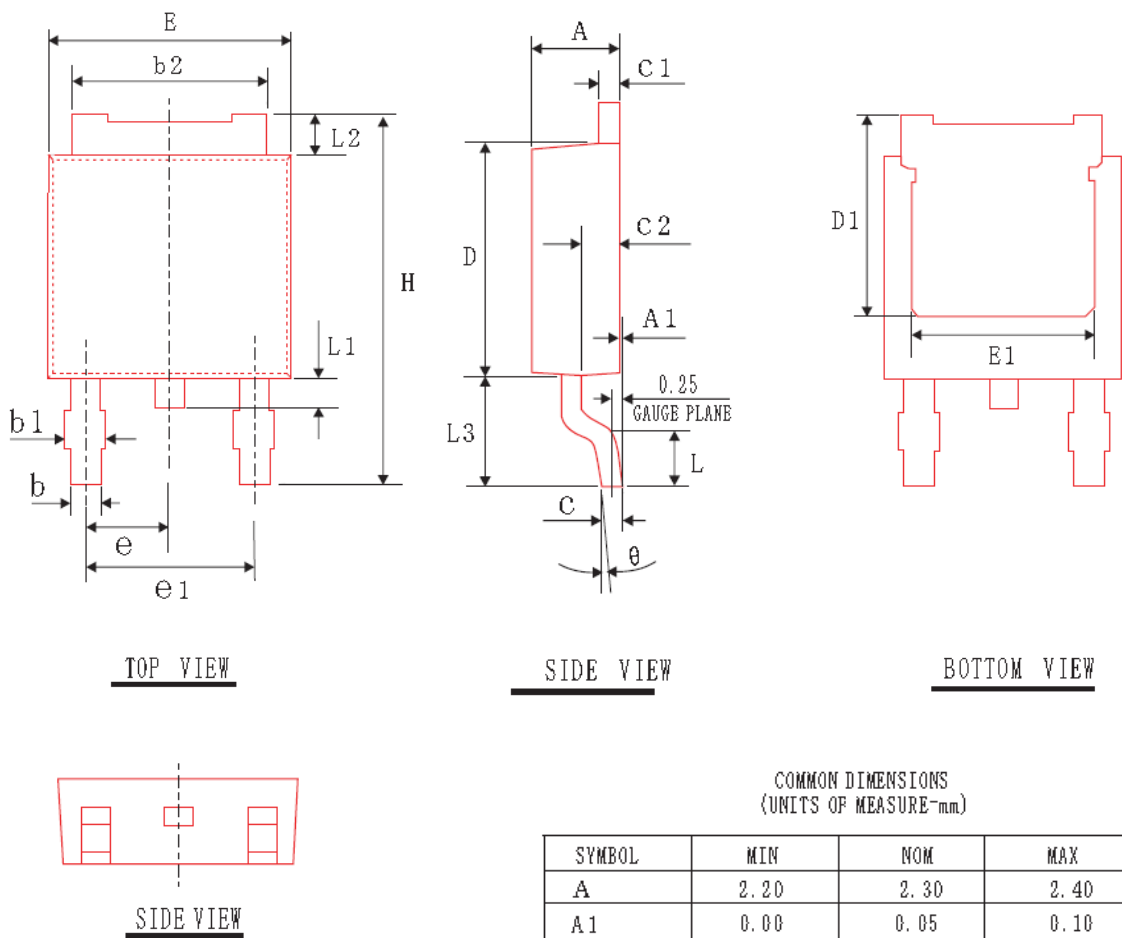


Figure 14. Switching times with waveform



CE65H450TOEI

PACKAGE DIMENSIONS



COMMON DIMENSIONS (UNITS OF MEASURE-mm)			
SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	0.05	0.10
b	0.762	0.812	0.862
b1	---	---	1.10
b2	5.23	5.33	5.43
c	0.458	0.508	0.558
c1	0.458	0.508	0.558
c2	0.80	1.00	1.20
D	6.00	6.10	6.20
D1	5.25	5.45	5.65
H	10.00	10.10	10.20
E	6.50	6.60	6.70
E1	4.75	4.85	4.95
e1	4.37	4.57	4.77
L	---	---	1.45
L1	0.60	0.75	0.90
L2	0.90	1.10	1.30
L3	2.80	3.00	3.20
θ	0°	4°	8°
e	2.285 BSC		



CE65H450TOEI

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-05-06	Initial release
2.0	2025-01-02	Optimize application platform testing